CLAIMS

1. A programmable Digital Signal Processor comprising a digital filter, a Shift Register Lookup table and a filter memory, wherein said Shift Register Lookup table is coupled to provide input data to said digital filter in a first mode of operation, and said filter memory is coupled to provide filter coefficients to said digital filter in said first mode of operation, said programmable Digital Signal Processor being characterised by further comprising a state machine, said state machine providing addressing values to said Shift Register Lookup table and said filter memory, wherein said addressing values comprise a single address for said Shift Register Lookup table and said filter memory, whereby the values stored in said Shift Register Lookup table and said filter memory are structured such that said single address references said corresponding coefficients and input data for said digital filter in said first mode of operation ~~wherein the outputs of said filter memory and said Shift Register Lookup table are synchronized so as to produce corresponding filter coefficients and input data together implementing a desired filter configuration.~~

2. The programmable Digital Signal Processor of claim 1 wherein said Shift Register Lookup table comprises a shift register, wherein said shift register is configured so as to be operable either as a single continuous shift register, or as a plurality of independently operable shift registers.

~~3. The programmable Digital Signal Processor of claim 1 or 2 further comprising a state machine, said state machine providing addressing values to said Shift Register Lookup table and said filter memory.~~

~~4. The programmable Digital Signal Processor of claim 2 wherein said addressing values comprise a single address for said Shift Register Lookup table and said filter memory, whereby the values stored in said Shift Register Lookup table and said filter memory are structured such that said single~~

~~address references said corresponding coefficients and input data for said digital filter in said first mode of operation.~~

~~5~~3. The programmable Digital Signal Processor of any preceding claim wherein in a second mode of operation the values stored in said Shift Register Lookup table are output for processing other than by said digital filter.

~~6~~4. The programmable Digital Signal Processor of claim ~~5~~ 3 wherein in said second mode of operation said Shift Register Lookup table is used as a multiplier input register.

~~7~~5. The programmable Digital Signal Processor of any preceding claim wherein said digital filter constitutes a component of a Finite Impulse Response filter.

~~8~~6. The programmable Digital Signal Processor of any ~~of~~ preceding claim~~s 3 to 6~~ wherein said digital filter constitutes a component of an Infinite Impulse Response filter comprising a first Finite Impulse Response filter and a second Finite Impulse Response filter in a feedback configuration, where said state machine provides enabling signals coordinate the combination of the outputs of said first Finite Impulse Response filter and said second Finite Impulse Response filter to implement said Infinite Impulse Response filter.

~~9~~7. The programmable Digital Signal Processor of any preceding claim wherein said Digital Signal Processor is implemented in an FPGA architecture comprising a plurality of Lookup Tables, the configuration of each said Lookup table being defined by one or more respective memory units programmed at system initiation with a configuration bit stream, wherein the values in said filter memory are also programmed by said configuration bit stream.

~~10~~8. A method of performing Digital Signal Processor operation, said method comprising

addressing a Shift Register Lookup table to output data to said Digital Signal Processor in a first mode of operation, and addressing a filter memory to provide coefficients to ~~said~~ a digital filter in said first mode of operation, performing a digital filter operation on said input data using said coefficient, said ~~.~~

~~11. The~~ method ~~of claim 10~~being characterised by comprising the further step of structuring said Shift Register Lookup table and said filter memory such that a single address value references corresponding coefficients and input data for said digital filter in said first mode of operation, such that said steps of addressing a Shift Register Lookup table to output a coefficients to said Digital Signal Processor in a first mode of operation, and addressing a filter memory to provide input data to said digital filter in said first mode of operation are performed using said single address value.

~~12~~9. The method of claim ~~10 or 11~~8 wherein said digital filter operation is a Finite Impulse Response filter operation.

~~13~~10. The method of claim ~~11~~ 8 or ~~12~~ 9 wherein said digital filter operation is an Infinite Impulse Response filter operation comprising a first Finite Impulse Response operation and a second Finite Impulse Response operation based on feedback values, said method comprising the further step of providing enabling signals coordinating the combination of the results of said first Finite Impulse Response operation and said second Finite Impulse Response operation to obtain an Infinite Impulse Response filter result.

~~14~~11. A program for a computer comprising instructions adapted to implement the steps of any of claims ~~10~~ 8 to ~~13~~10.