

[Fig. 1]

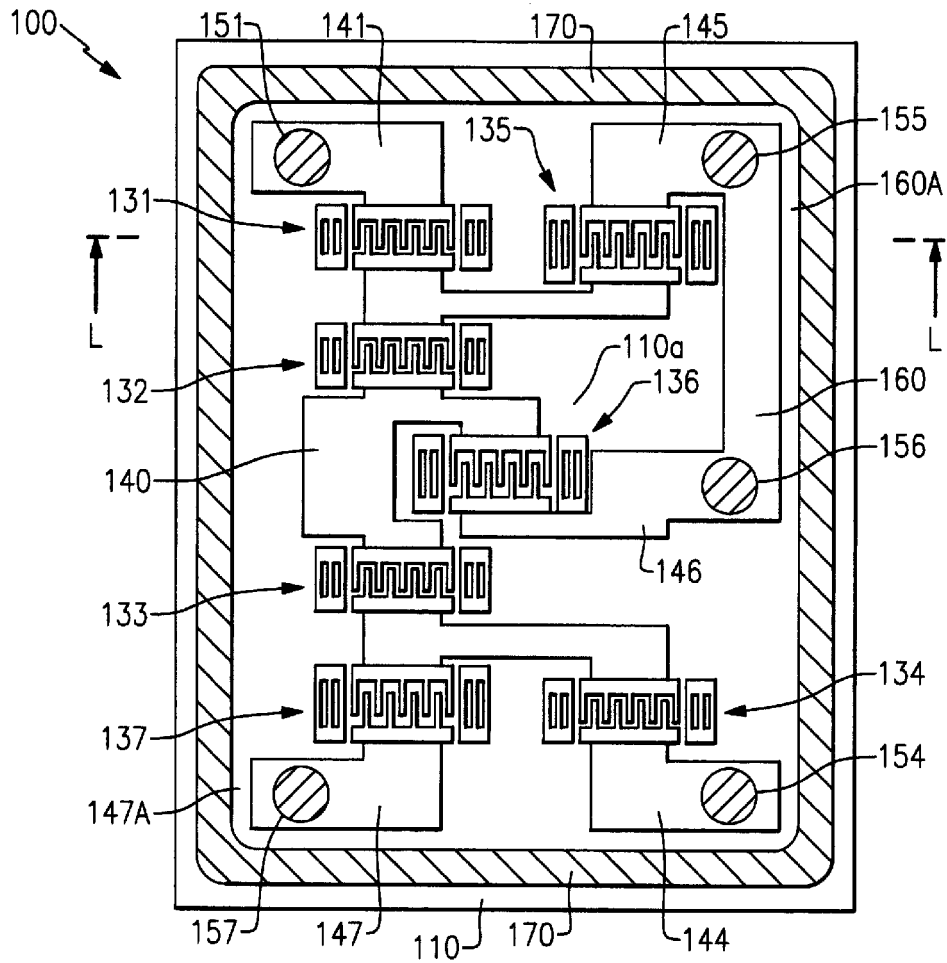


FIG. 1A
(RELATED ART)

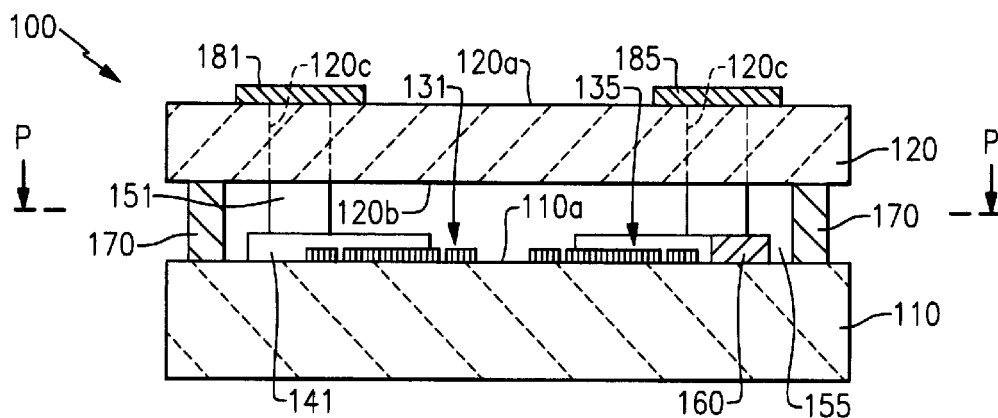
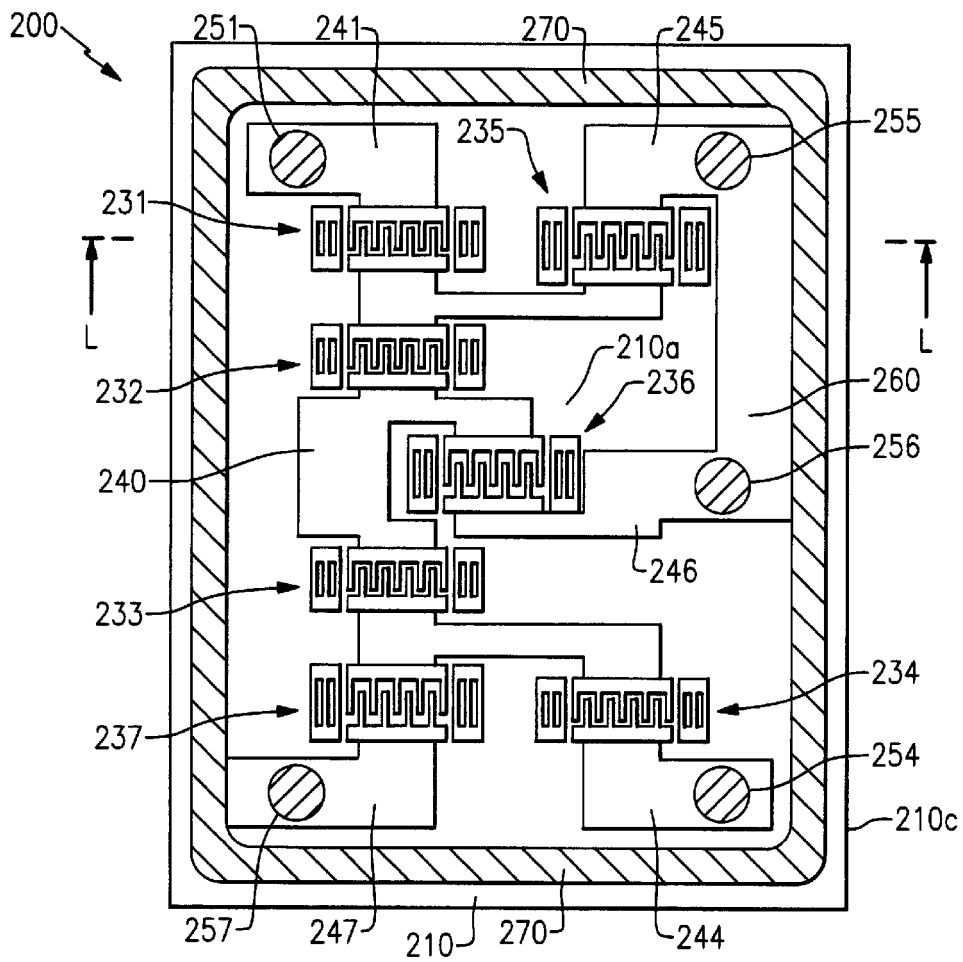
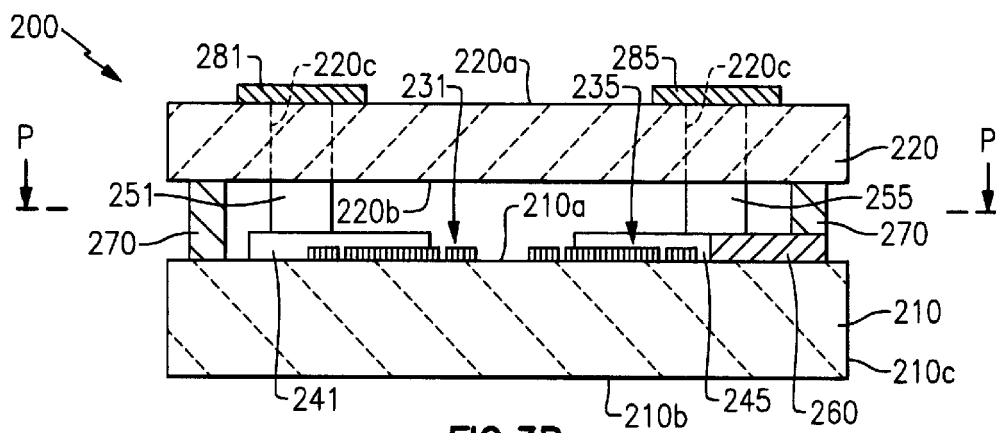


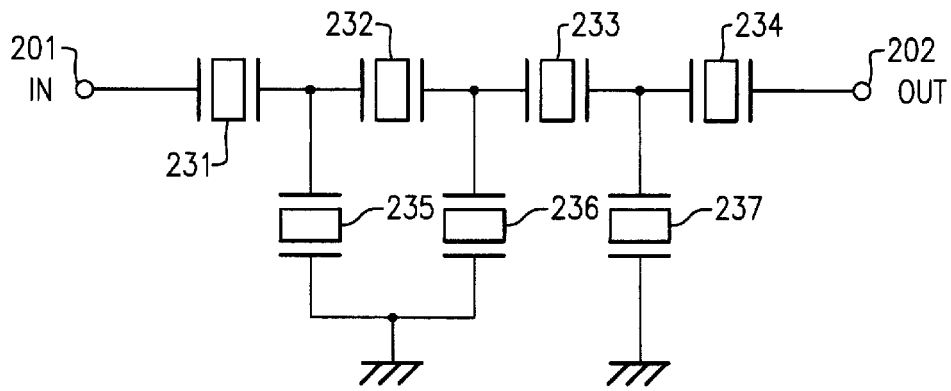
FIG. 1B
(RELATED ART)

FIG.2
(RELATED ART)

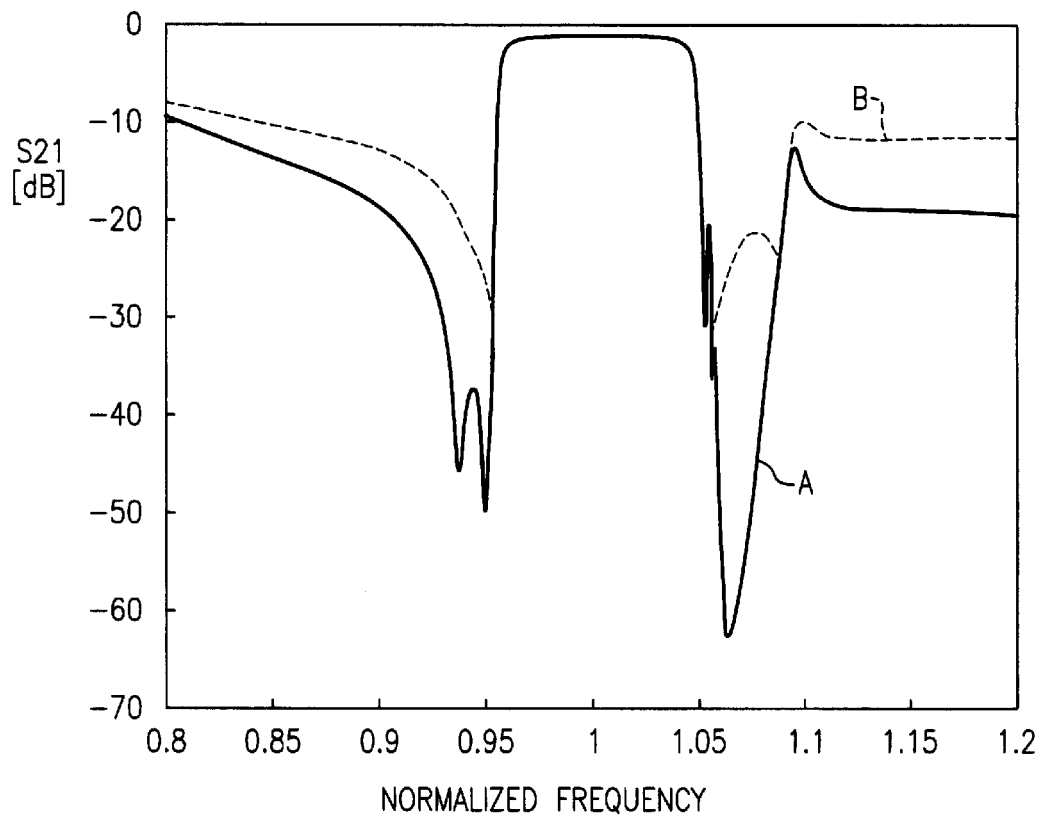
[Fig. 3]

**FIG. 3A****FIG. 3B**

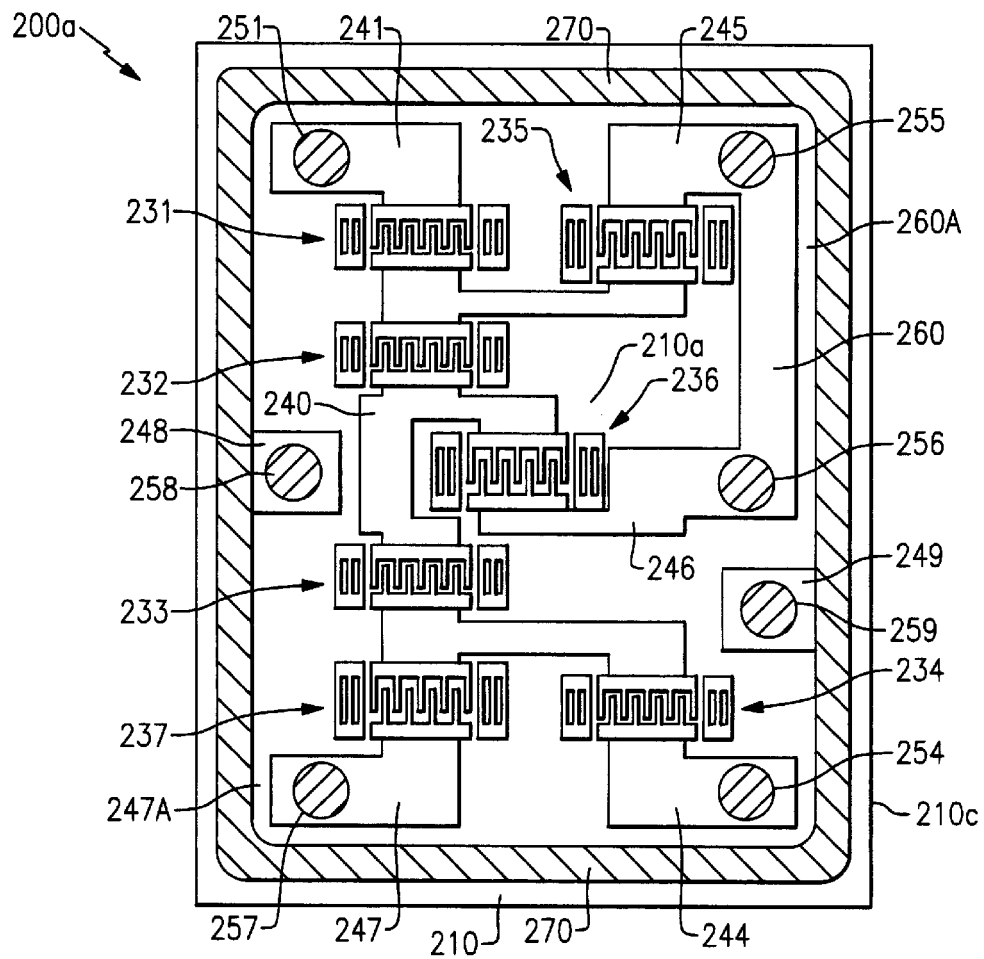
[Fig. 4]

**FIG.4**

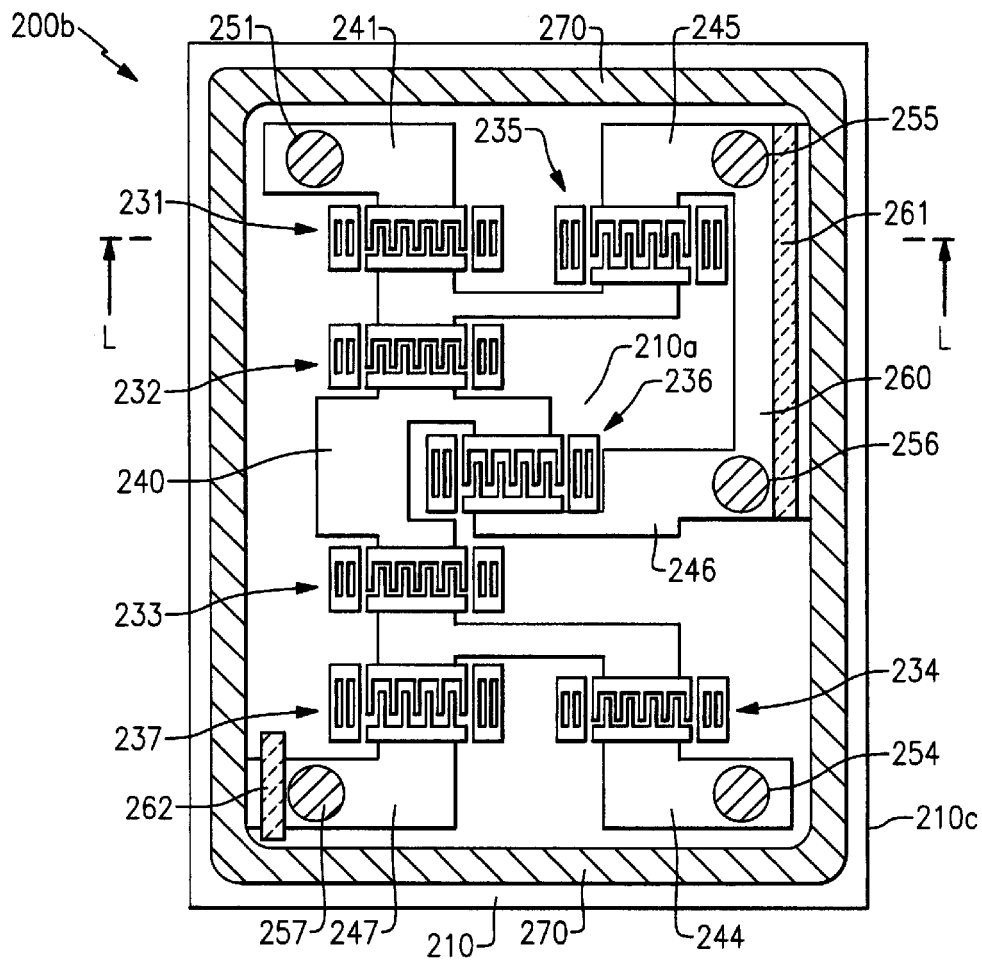
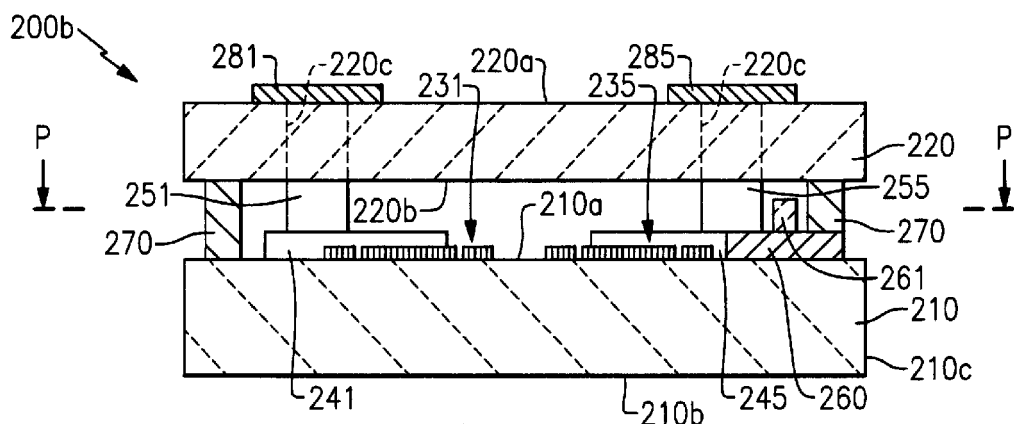
[Fig. 5]

**FIG.5**

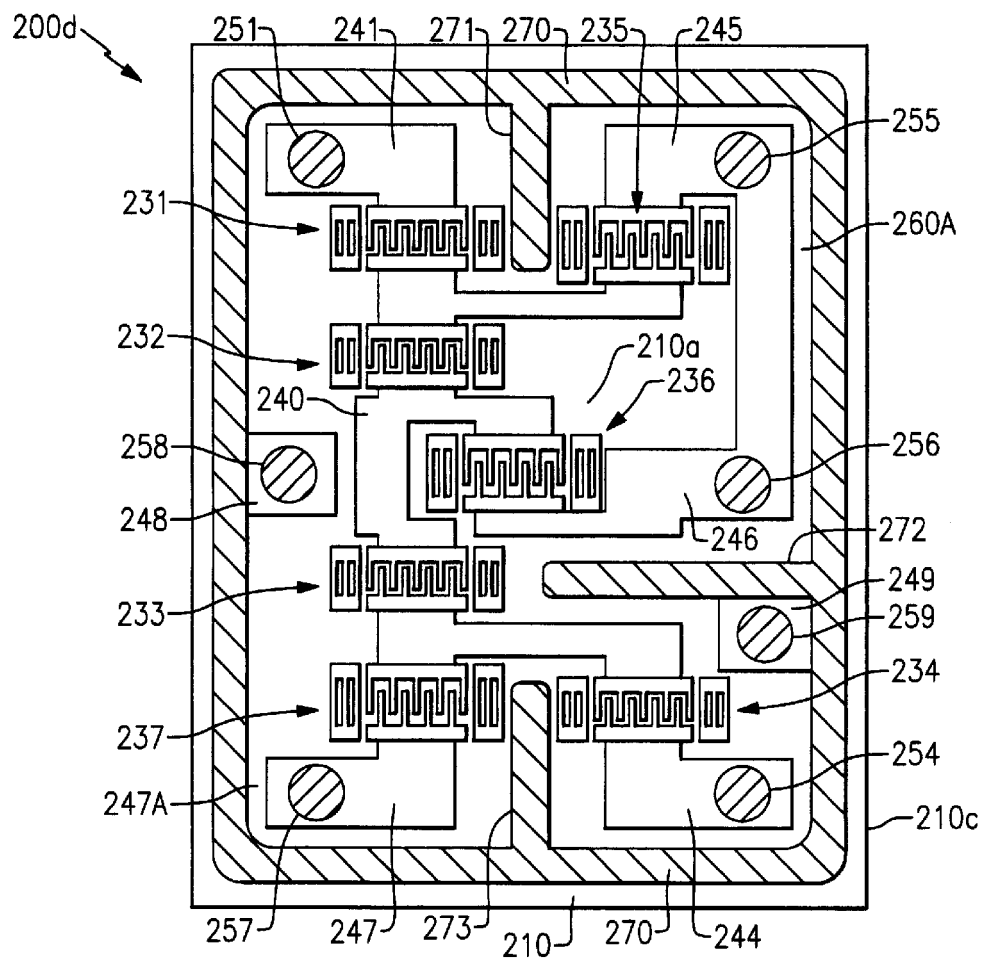
[Fig. 6]

**FIG. 6**

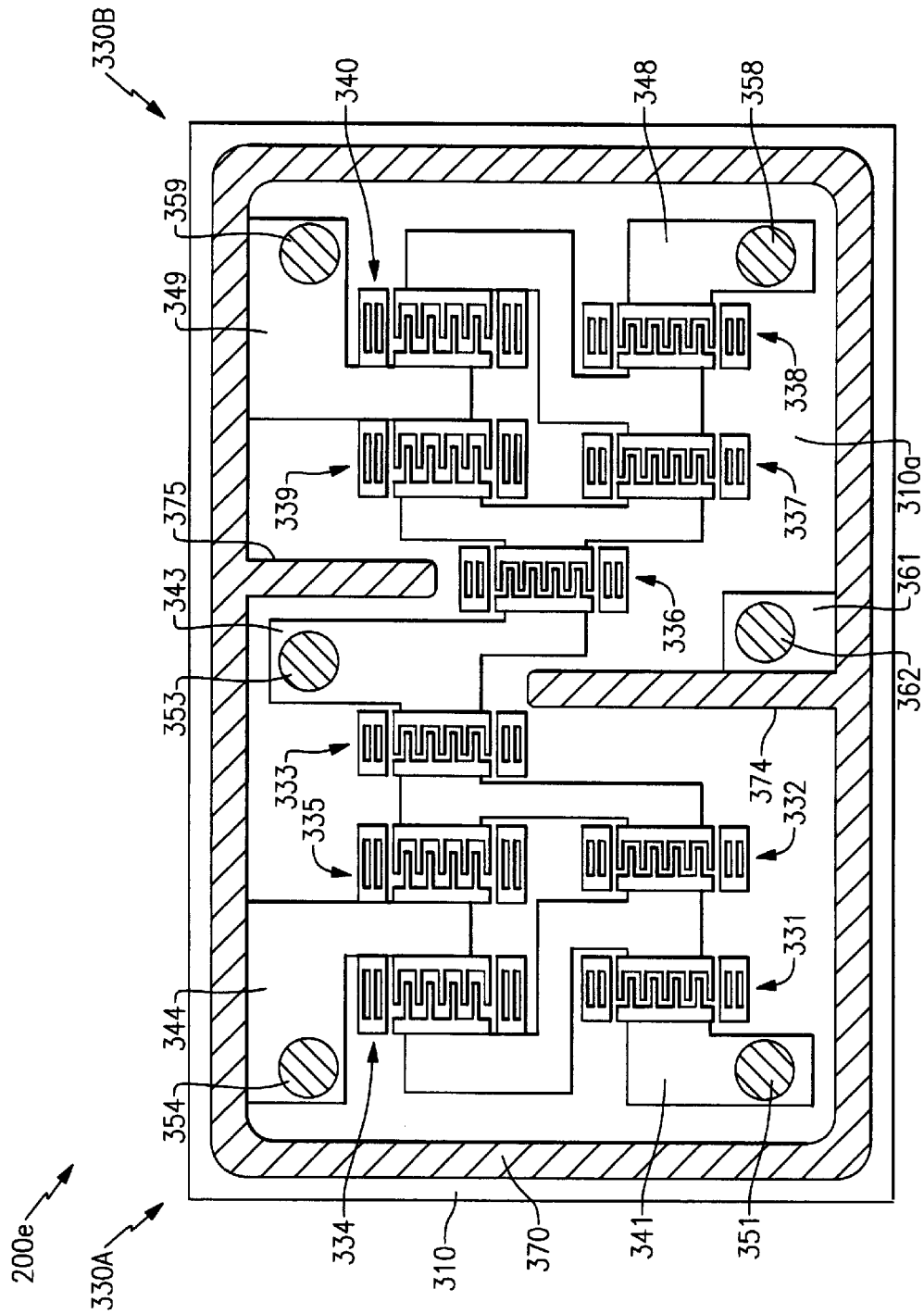
[Fig. 7]

**FIG. 7A****FIG. 7B**

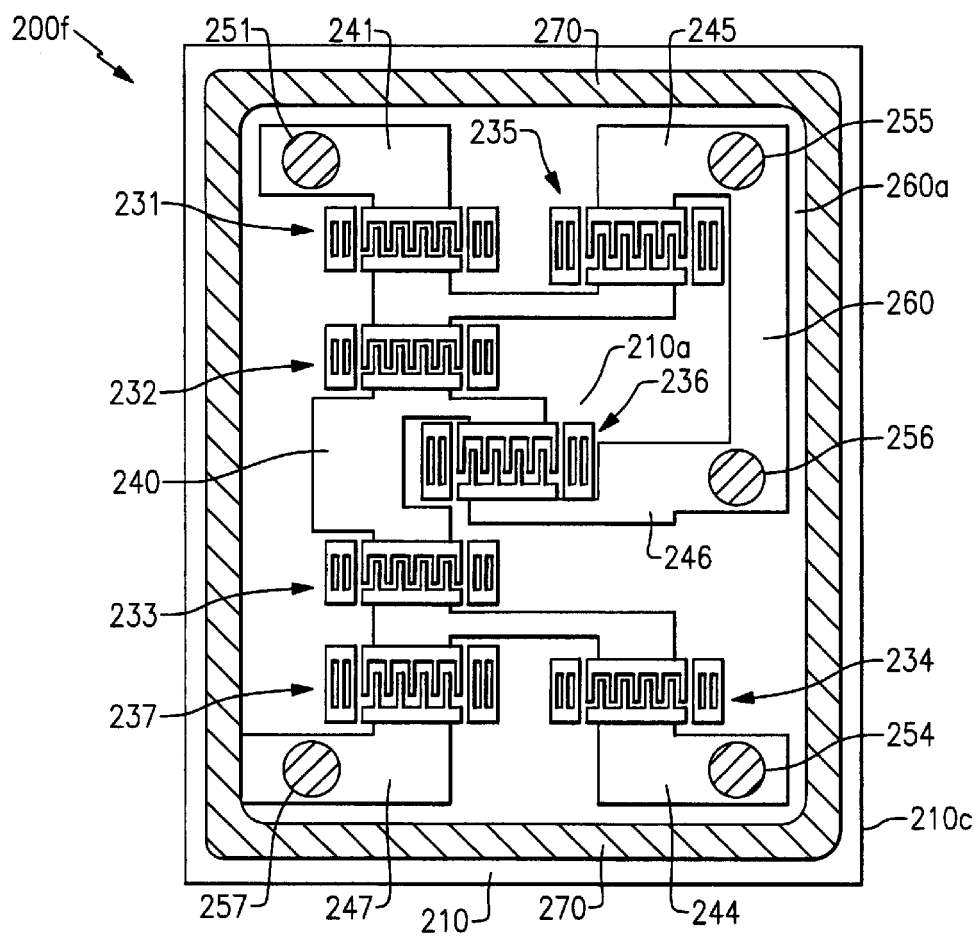
[Fig. 9]

**FIG. 9**

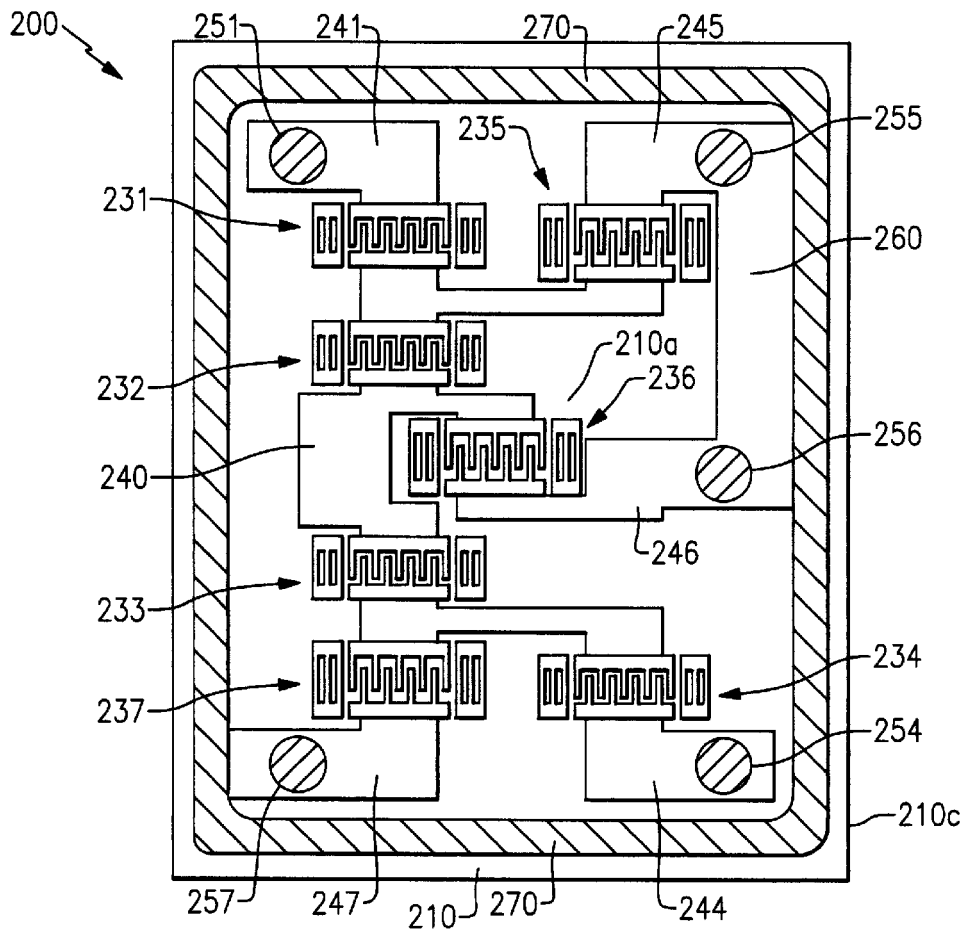
[Fig. 10]

**FIG. 10**

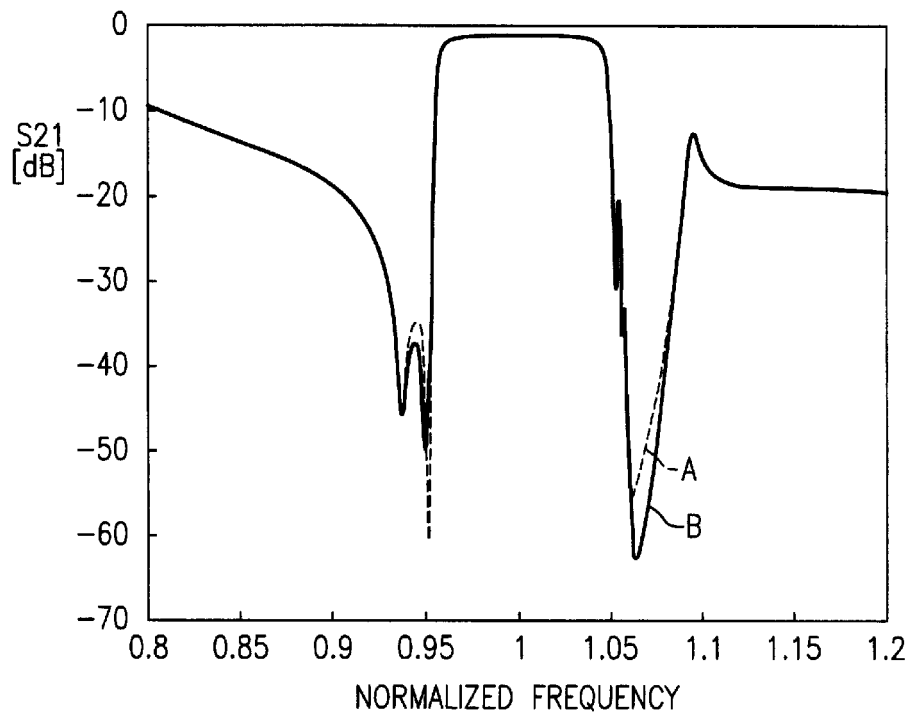
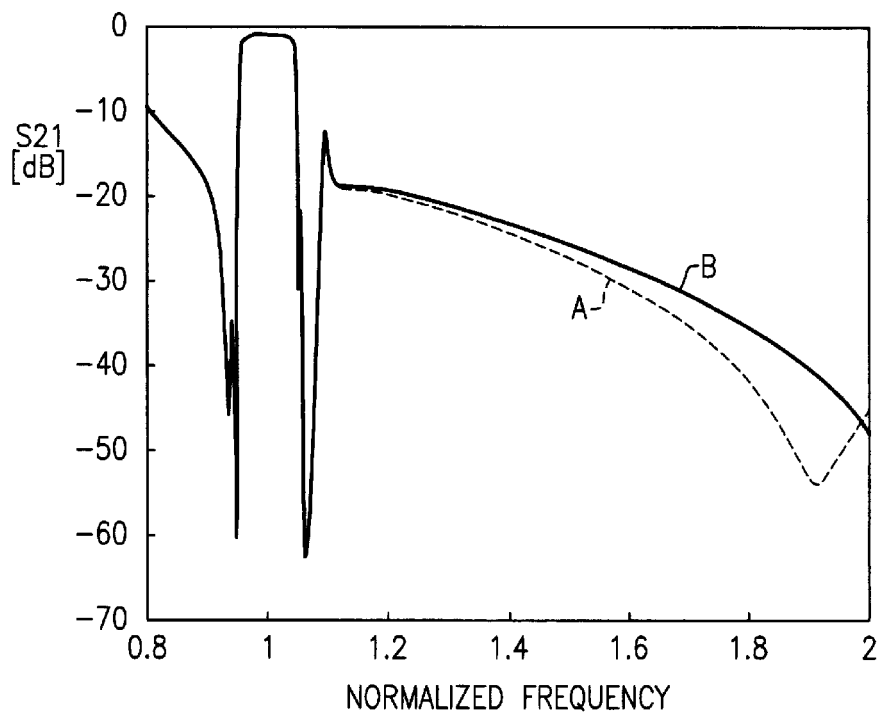
[Fig. 11A]

**FIG. 11A**

[Fig. 11B]

**FIG.11B**

[Fig. 12]

**FIG.12A****FIG.12B**

[illegible][illegible]

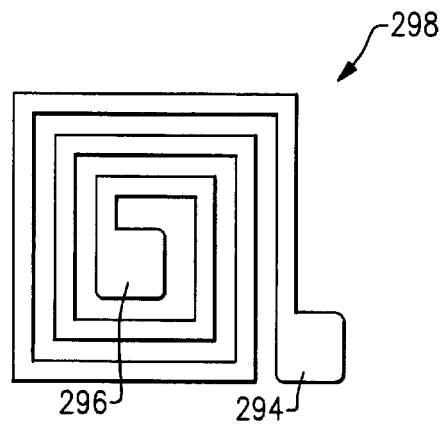
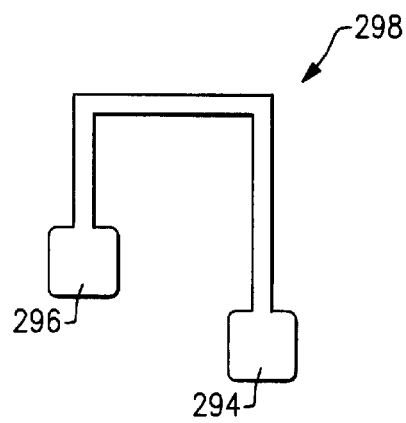
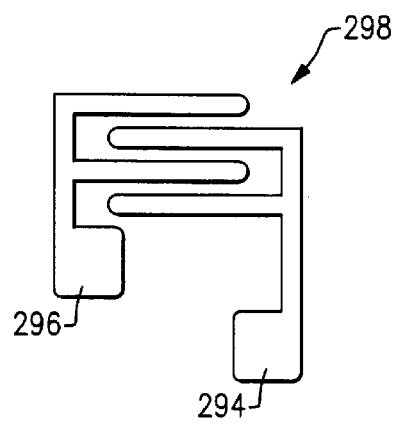
FIG.15

A cross-sectional view of a semiconductor device 200j. The device consists of a substrate 210 with a top layer 210a and a bottom layer 210b. A central layer 252 is positioned between the top and bottom layers. On the top layer 210a, there are three rectangular regions 220c, each containing a smaller rectangular region 220a. These regions are separated by a layer 231. The top layer 210a is covered by a layer 241. The bottom layer 210b is covered by a layer 245. The central layer 252 is covered by a layer 270. The device is labeled 200j in the top left corner.

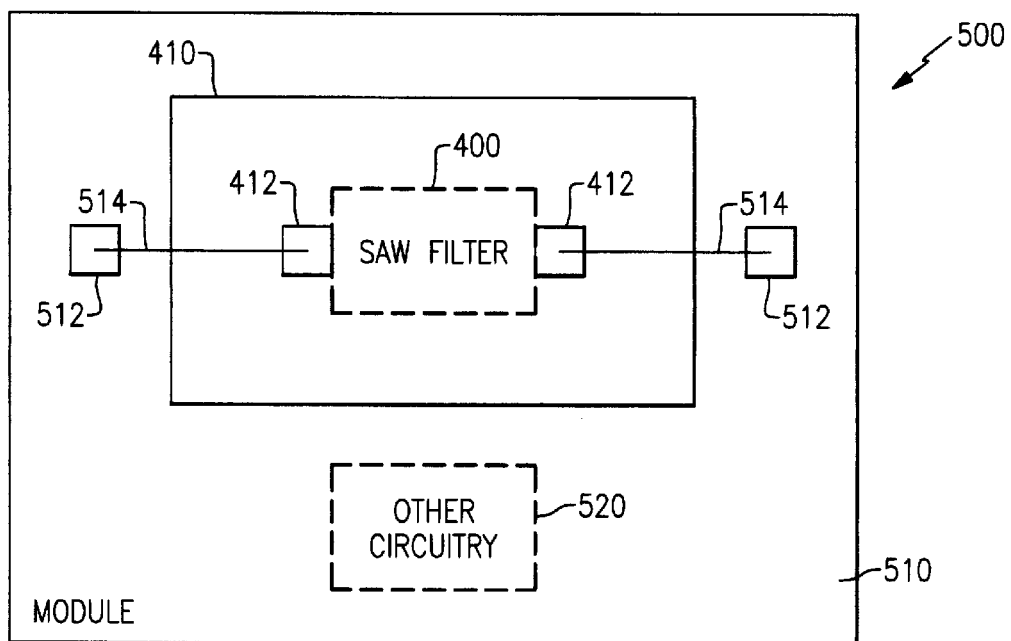
[illegible]

FIG.17

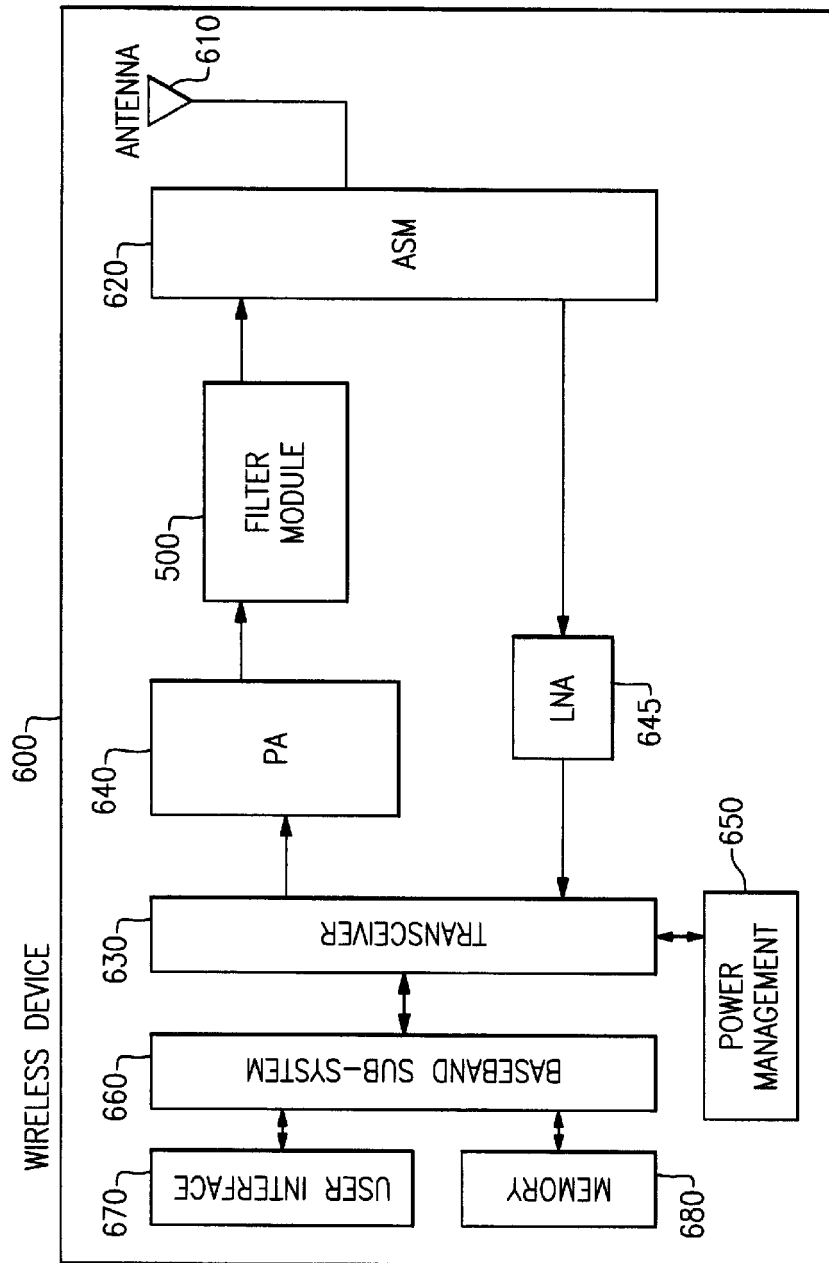
[Fig. 18]

**FIG. 18A****FIG. 18B****FIG. 18C**

[Fig. 19]

**FIG.19**

[Fig. 20]

FIG.20