

Process for Improving Copper Line Cap Formation

ABSTRACT OF THE DISCLOSURE

An integrated circuit includes a semiconductor substrate, a low-k dielectric layer over the semiconductor substrate, a first opening in the low-k dielectric layer, and a first diffusion barrier layer in the first opening covering the low-k dielectric layer in the first opening, wherein the first diffusion barrier layer has a bottom portion connected to sidewall portions, and wherein the sidewall portions have top surfaces close to a top surface of the low-k dielectric layer. The integrated circuit further includes a conductive line filling the first opening wherein the conductive line has a top surface lower than the top surfaces of the sidewall portions of the diffusion barrier layer, and a metal cap on the conductive line and only within a region directly over the conductive line.

Figure 7a