

Abstract of the Disclosure

A set of N digital data bits serially supplied to an input node are converted to an analog voltage by means of N binary weighted capacitors and N switching transistors, one capacitor being associated with one switching transistor for each one of the N digital data bits. Each capacitor is connected between an output node and via the conduction path of its associated switching transistor to a first power terminal. Two transistors are used to selectively sample the N bits of serial data and to couple and store the sampled data on the gates of the switching transistors which are precharged so that the two transistors coupling the serial data only need to conduct in the common source mode. The serial data applied to the gates of the switching transistor is transferred to the N capacitors when a charging voltage is applied to the output node. Following the data transfer onto the binary weighted capacitors, the switching transistors are precharged and, concurrently the N capacitors are connected in parallel to produce an analog voltage corresponding to the serial data.

This Sheet Has Been Replaced

