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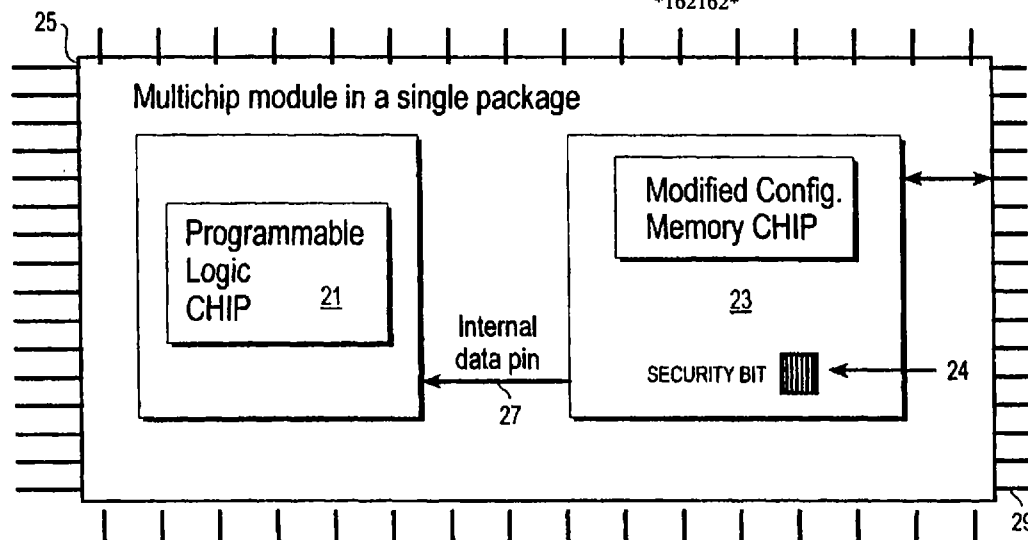
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(54) Title: SECURE PROGRAMMABLE LOGIC DEVICE



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(57) Abstract: A programmable logic chip (21) and configuration memory chip (23) are mounted within a multi-chip module (25) to form a single package. The configuration memory has a security bit (24) which in a first state allows programming a read-back of configuration data in the memory chip via external pins (29) of the package, and in a second state allows only erase command to be communicated to the memory chip via the external pins. The internal data transfer connection (27) between the memory chip and programmable logic chip is enabled when the security bit is in the second state and the memory chip is in a read-back mode, allowing configuration data to be loaded into the logic chip upon power up.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.