**Claims**

1. A transistor arrangement, comprising:

a nanowire comprising a first nanowire region and a second nanowire region;

a first gate contact disposed over the first nanowire region;

an insulating region disposed over the second nanowire region;

a second gate contact disposed over the insulating region;

wherein the first nanowire region and the first gate contact forms a part of an enhancement mode transistor and the second nanowire region, the insulating region and the second gate contact forms a part of a depletion mode transistor.

2. The transistor arrangement of claim 1, further comprising

a first source contact and a first drain contact respectively disposed in connection with or over the first nanowire region such that the first gate contact is positioned between the first source contact and the first drain contact.

3. The transistor arrangement of claim 1 or 2, further comprising

a second source contact and a second drain contact respectively disposed in connection with or over the second nanowire region such that the second gate contact is positioned between the second source contact and the second drain contact.

4. The transistor arrangement of any one of claims 1 to 3,

wherein the first gate contact and the first nanowire region form a schottky contact.

5. The transistor arrangement of any one of claims 2 to 4,

wherein the first source contact and the first nanowire region form an ohmic contact and the first drain contact and the first nanowire region form a further ohmic contact.

6. The transistor arrangement of any one of claims 1 to 5,

wherein the insulating region is configured to substantially surround the second nanowire region.

7. The transistor arrangement of any one of claims 1 to 6,

wherein the second nanowire region is positioned adjacent to the first nanowire region.

8. The transistor arrangement of any one of claims 1 to 7, further comprising

a support substrate,

wherein the nanowire is positioned above and spaced at a distance away from the support substrate.

9. The transistor arrangement of any one of claims 1 to 8,

wherein the nanowire comprises a material selected from a group consisting of ZnO, $SnO_2$, $TiO_2$, GaN, InO.

10. The transistor arrangement of any one of claims 3 to 9,

wherein each of the first source contact, the first gate contact, the first drain contact, the second source contact, the second gate contact, the second drain contact comprises a metal material selected from a group consisting of Pt, Au, Pd, Ir, Ni.

11. The transistor arrangement of any one of claims 1 to 10,

wherein the insulating region comprises a material selected from a group consisting of $SiO_2$, $Al_2O_3$, $TiO_2$, $HfO_2$.

12. The transistor arrangement of any one of claims 2 to 11,

wherein the first source contact is coupled to a ground potential.

13. The transistor arrangement of any one of claims 1 to 12,

wherein the first gate contact is coupled to a voltage input of the transistor arrangement.

14. The transistor arrangement of any one of claims 3 to 13,

wherein the first drain contact is coupled to the second source contact.

15. The transistor arrangement of any one of claims 1 to 14,

wherein the second gate contact is coupled to a voltage output of the transistor arrangement.

16. The transistor arrangement of any one of claims 3 to 15,

wherein the second drain contact is coupled to a supply voltage.

17. The transistor arrangement of any one of claims 3 to 16,

wherein the second gate contact is further coupled to the first drain contact and the second source contact.

18. The transistor arrangement of any one of claims 1 to 17,

wherein the enhancement mode transistor forms a driver of the transistor arrangement.

19. The transistor arrangement of any one of claims 1 to 18,

wherein the depletion mode transistor forms a load of the transistor arrangement.

20. The transistor arrangement of any one of claims 1 to 19,

wherein the transistor arrangement is configured as a direct-coupled field-effect transistor logic inverter.

21. A method of forming a transistor arrangement, the method comprising:

forming a nanowire comprising a first nanowire region and a second nanowire region over a support substrate;

forming a first gate contact over the first nanowire region;

forming an insulating region over the second nanowire region;

forming a second gate contact over the insulating region;

wherein forming the first nanowire region and the first gate contact forms a part of forming an enhancement mode transistor and forming the second nanowire region, the insulating region and the second gate contact forms a part of forming a depletion mode transistor.

22. The method of claim 21, further comprising

forming a first source contact and a first drain contact respectively in connection with or over the first nanowire region such that the first gate contact is formed between the first source contact and the first drain contact.

23. The method of claim 21 or 22, further comprising

forming a second source contact and a second drain contact respectively in connection with or over the second nanowire region such that the second gate contact is formed between the second source contact and the second drain contact.

24. The method of any one of claims 21 to 23,

wherein forming the first gate contact over the first nanowire region comprises forming a schottky contact between the first gate contact and the first nanowire region.

25. The method of any one of claims 22 to 24,

wherein forming the first source contact in connection with or over the first nanowire region comprises forming an ohmic contact between the first source contact and the first nanowire region and wherein forming the first drain contact in connection with or over the first nanowire region comprises forming a further ohmic contact between the first drain contact and the first nanowire region.

26. The method of any one of claims 21 to 25,

wherein forming the insulating region over the second nanowire region comprises forming the insulating region such that the insulating region is configured to substantially surround the second nanowire region.

27. The method of any one of claims 21 to 26,

wherein forming the nanowire comprises forming the second nanowire region adjacent to the first nanowire region.

28. The method of any one of claims 21 to 27,

wherein forming the nanowire over the support substrate comprises forming the nanowire above and at a distance away from the support substrate.

29. The method of any one of claims 21 to 28,

wherein forming the first gate contact over the first nanowire region comprises direct writing of a metal electrode onto the first nanowire region.

30. The method of claim 29,

wherein direct writing of the metal electrode onto the first nanowire region comprises writing using a focused electron beam or a focused ion beam.

31. The method of any one of claims 21 to 30,

wherein forming the insulating region over the second nanowire region comprises direct writing of a dielectric layer onto the second nanowire region.

32. The method of claim 31,

wherein direct writing of the dielectric layer onto the second nanowire region comprises writing using a focused electron beam or a focused ion beam.

33. The method of any one of claims 21 to 32,

wherein forming the second gate contact over the insulating region comprises direct writing of a metal electrode onto the insulating region.

34. The method of claim 33,

wherein direct writing of the metal electrode onto the insulating region comprises writing using a focused electron beam or a focused ion beam.

35. The method of claim 29 or 33,

wherein the metal electrode comprises a material selected from a group of materials consisting of Pt, Au, Pd, Ir, Ni.

36. The method of claim 31,

wherein the dielectric layer comprises a material selected from a group of materials consisting of $SiO_2$, $Al_2O_3$, $TiO_2$, $HfO_2$.

37. The method of any one of claims 22 to 36,

wherein forming the first source contact and the first drain contact respectively in connection with or over the first nanowire region comprises direct writing of respective metal electrodes onto the first nanowire region.

38. The method of any one of claims 23 to 37,

wherein forming the second source contact and the second drain contact respectively in connection with or over the second nanowire region comprises direct writing of respective metal electrodes onto the second nanowire region.

39. A method of forming a transistor, the method comprising:

forming a nanowire over a support substrate; and

forming a gate contact directly onto a region of the nanowire;

wherein the gate contact is formed by directly writing a metal electrode onto the region of the nanowire using focused electron beam.

40. The method of claim 39,

wherein forming the gate contact directly onto the region of the nanowire comprises forming a schottky contact between the gate contact and the region of the nanowire.

41. A method of forming a transistor, the method comprising:

forming a nanowire over a support substrate;

forming a gate contact;

forming an insulating region between a region of the nanowire and the gate contact;

wherein the gate contact is formed by directly writing a metal electrode onto the insulating region;

wherein the insulating region is formed by directly writing a dielectric layer onto the region of the nanowire using focused electron beam.

42. A transistor, comprising:

a nanowire; and

a gate contact directly written onto a region of the nanowire using focused electron beam.

43. The transistor of claim 42,

wherein the transistor is configured as an enhancement mode transistor.

44. A transistor, comprising:

a nanowire;

a gate contact; and

an insulating region positioned between a region of the nanowire and the gate contact;

wherein the gate contact is directly written onto the insulating region;

wherein the insulating region is directly written onto the region of the nanowire using focused electron beam.

45. The transistor of claim 44,

wherein the transistor is configured as a depletion mode transistor.

## Claims

1. A transistor arrangement, comprising:

a nanowire comprising a first nanowire region and a second nanowire region;

a first gate contact disposed over the first nanowire region;

an insulating region disposed over the second nanowire region;

a second gate contact disposed over the insulating region;

wherein the first nanowire region and the first gate contact forms a part of an enhancement mode transistor and the second nanowire region, the insulating region and the second gate contact forms a part of a depletion mode transistor.

2. The transistor arrangement of claim 1, further comprising

a first source contact and a first drain contact respectively disposed in connection with or over the first nanowire region such that the first gate contact is positioned between the first source contact and the first drain contact.

3. The transistor arrangement of claim 1 or 2, further comprising

a second source contact and a second drain contact respectively disposed in connection with or over the second nanowire region such that the second gate contact is positioned between the second source contact and the second drain contact.

4. The transistor arrangement of any one of claims 1 to 3,

wherein the first gate contact and the first nanowire region form a schottky contact.

5. The transistor arrangement of any one of claims 2 to 4,

wherein the first source contact and the first nanowire region form an ohmic contact and the first drain contact and the first nanowire region form a further ohmic contact.

6. The transistor arrangement of any one of claims 1 to 5,

wherein the insulating region is configured to substantially surround the second nanowire region.

7. The transistor arrangement of any one of claims 1 to 6,

wherein the second nanowire region is positioned adjacent to the first nanowire region.

8. The transistor arrangement of any one of claims 1 to 7, further comprising

a support substrate,

wherein the nanowire is positioned above and spaced at a distance away from the support substrate.

9. The transistor arrangement of any one of claims 1 to 8,

wherein the nanowire comprises a material selected from a group consisting of ZnO, $SnO_2$, $TiO_2$, GaN, InO.

10. The transistor arrangement of any one of claims 3 to 9,

wherein each of the first source contact, the first gate contact, the first drain contact, the second source contact, the second gate contact, the second drain contact comprises a metal material selected from a group consisting of Pt, Au, Pd, Ir, Ni.

11. The transistor arrangement of any one of claims 1 to 10,

wherein the insulating region comprises a material selected from a group consisting of $SiO_2$, $Al_2O_3$, $TiO_2$, $HfO_2$.

12. The transistor arrangement of any one of claims 2 to 11,

wherein the first source contact is coupled to a ground potential.

13. The transistor arrangement of any one of claims 1 to 12,

wherein the first gate contact is coupled to a voltage input of the transistor arrangement.

14. The transistor arrangement of any one of claims 3 to 13,

wherein the first drain contact is coupled to the second source contact.

15. The transistor arrangement of any one of claims 1 to 14,

wherein the second gate contact is coupled to a voltage output of the transistor arrangement.

16. The transistor arrangement of any one of claims 3 to 15,

wherein the second drain contact is coupled to a supply voltage.

17. The transistor arrangement of any one of claims 3 to 16,

wherein the second gate contact is further coupled to the first drain contact and the second source contact.

18. The transistor arrangement of any one of claims 1 to 17,

wherein the enhancement mode transistor forms a driver of the transistor arrangement.

19. The transistor arrangement of any one of claims 1 to 18,

wherein the depletion mode transistor forms a load of the transistor arrangement.

20. The transistor arrangement of any one of claims 1 to 19,

wherein the transistor arrangement is configured as a direct-coupled field-effect transistor logic inverter.

21. A method of forming a transistor arrangement, the method comprising:

forming a nanowire comprising a first nanowire region and a second nanowire region over a support substrate;

forming a first gate contact over the first nanowire region;

forming an insulating region over the second nanowire region;

forming a second gate contact over the insulating region;

wherein forming the first nanowire region and the first gate contact forms a part of forming an enhancement mode transistor and forming the second nanowire region, the insulating region and the second gate contact forms a part of forming a depletion mode transistor.

22. The method of claim 21, further comprising

forming a first source contact and a first drain contact respectively in connection with or over the first nanowire region such that the first gate contact is formed between the first source contact and the first drain contact.

23. The method of claim 21 or 22, further comprising

forming a second source contact and a second drain contact respectively in connection with or over the second nanowire region such that the second gate contact is formed between the second source contact and the second drain contact.

24. The method of any one of claims 21 to 23,

wherein forming the first gate contact over the first nanowire region comprises forming a schottky contact between the first gate contact and the first nanowire region.

25. The method of any one of claims 22 to 24,

wherein forming the first source contact in connection with or over the first nanowire region comprises forming an ohmic contact between the first source contact and the first nanowire region and wherein forming the first drain contact in connection with or over the first nanowire region comprises forming a further ohmic contact between the first drain contact and the first nanowire region.

26. The method of any one of claims 21 to 25,

wherein forming the insulating region over the second nanowire region comprises forming the insulating region such that the insulating region is configured to substantially surround the second nanowire region.

27. The method of any one of claims 21 to 26,

wherein forming the nanowire comprises forming the second nanowire region adjacent to the first nanowire region.

28. The method of any one of claims 21 to 27,

wherein forming the nanowire over the support substrate comprises forming the nanowire above and at a distance away from the support substrate.

29. The method of any one of claims 21 to 28,

wherein forming the first gate contact over the first nanowire region comprises direct writing of a metal electrode onto the first nanowire region.

30. The method of claim 29,

wherein direct writing of the metal electrode onto the first nanowire region comprises writing using a focused electron beam or a focused ion beam.

31. The method of any one of claims 21 to 30,

wherein forming the insulating region over the second nanowire region comprises direct writing of a dielectric layer onto the second nanowire region.

32. The method of claim 31,

wherein direct writing of the dielectric layer onto the second nanowire region comprises writing using a focused electron beam or a focused ion beam.

33. The method of any one of claims 21 to 32,

wherein forming the second gate contact over the insulating region comprises direct writing of a metal electrode onto the insulating region.

34. The method of claim 33,

wherein direct writing of the metal electrode onto the insulating region comprises writing using a focused electron beam or a focused ion beam.

35. The method of claim 29 or 33,

wherein the metal electrode comprises a material selected from a group of materials consisting of Pt, Au, Pd, Ir, Ni.

36. The method of claim 31,

wherein the dielectric layer comprises a material selected from a group of materials consisting of $SiO_2$, $Al_2O_3$, $TiO_2$, $HfO_2$.

37. The method of any one of claims 22 to 36,

wherein forming the first source contact and the first drain contact respectively in connection with or over the first nanowire region comprises direct writing of respective metal electrodes onto the first nanowire region.

38. The method of any one of claims 23 to 37,

wherein forming the second source contact and the second drain contact respectively in connection with or over the second nanowire region comprises direct writing of respective metal electrodes onto the second nanowire region.