VOLTAGE PULSE TIME-DOMAIN MULTIPLEXING

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to a system used in semiconductor device manufacturing. More specifically, embodiments of the present disclosure relate to a plasma processing system used to process a substrate.

Description of the Related Art

[0002] Reliably producing high aspect ratio features is one of the key technology challenges for the next generation of semiconductor devices. One method of forming high aspect ratio features uses a plasma-assisted etching process to bombard a material formed on a surface of a substrate through openings formed in a patterned mask layer formed on the substrate surface.

[0003] With technology nodes advancing towards 2nm, the fabrication of smaller features with larger aspect ratios requires atomic precision for plasma processing. For etching processes where the plasma ions play a major role, ion energy control is always challenging the development of reliable and repeatable device formation processes in the semiconductor equipment industry. In a typical plasma-assisted etching process, the substrate is positioned on an electrostatic chuck (ESC) disposed in a processing chamber, a plasma is formed over the substrate, and ions are accelerated from the plasma towards the substrate across a plasma sheath, i.e., region depleted of electrons, formed between the plasma and the surface of the substrate. Traditionally RF substrate biasing methods, which use sinusoidal RF waveforms to excite the plasma and form the plasma sheath, have been unable to desirably form these smaller device feature sizes. Recently, it has been found that the delivery of high voltage pulses to one or more electrodes within a processing chamber can be useful in desirably controlling the plasma sheath formed over the surface of the substrate. However, producing moderate to high frequency high voltage pulses is challenging. Such pulse may be especially difficult to produce using standard electrical components due to the heating of switching components used to form the high voltage pulses.

[0004] Accordingly, there is a need in the art for pulsed voltage source and biasing methods that are able to enable the completion of a desirable plasma-assisted process on a substrate.

SUMMARY

[0005] Embodiments provided herein generally include apparatus, plasma processing systems and methods for generation of a waveform for plasma processing of a substrate in a processing chamber.

[0006] One embodiment of the present disclosure is directed to a waveform generator for plasma processing. The waveform generator generally includes: voltage source circuitry; a first switch coupled between the voltage source circuitry and a first output node of the waveform generator, the first output node being configured to be coupled to a chamber; a second switch coupled between the first output node and electrical ground node; a third switch coupled between the voltage source circuitry and a second output node of the waveform generator, the second output node being configured to be coupled to the chamber; and a fourth switch coupled between the second output node and the electrical ground node.

[0007] One embodiment of the present disclosure is directed to a method for waveform generation. The method generally includes: coupling, via a first switch, voltage source circuitry to a first output node of a waveform generator, the first output node being coupled to a chamber; coupling, via a second switch, the first output node to an electrical ground node; coupling, via a third switch, the voltage source circuitry to a second output node of the waveform generator, the second output node being coupled to the chamber; and coupling, via a fourth switch, the second output node to the electrical ground node.

[0008] One embodiment of the present disclosure is directed to an apparatus for waveform generation. The apparatus generally includes voltage source circuitry, one or more switches coupled to the voltage source circuitry, and a controller configured to control the one or more switches. The one or more switches includes: a first switch coupled between the voltage source circuitry and a first output node of the waveform generator, the first output node being configured to be coupled to a chamber; a second switch coupled between the first output node and electrical ground node; a third switch

coupled between the voltage source circuitry and a second output node of the waveform generator, the second output node being configured to be coupled to the chamber; and a fourth switch coupled between the second output node and the electrical ground node.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above -recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope and may admit to other equally effective embodiments.

[0010] FIG. 1 is a schematic cross-sectional view of a processing system, according to one or more embodiments, configured to practice the methods set forth herein.

[0011] FIG. 2A illustrates a voltage waveform that is established on a substrate due to a voltage waveform applied to an electrode of a processing chamber.

[0012] FIG. 2B illustrates the effect of increasing plasma density on a voltage waveform that is established on a substrate due to a voltage waveform applied to an electrode of a processing chamber.

[0013] FIG. 2C illustrates the effect on an ion energy distribution (IED) associated with the effect of increasing plasma density that is illustrated in relation to the voltage waveform of FIG. 2B.

[0014] FIG. 3 illustrates an example waveform generated using time multiplexing of voltage pulses, in accordance with certain embodiments of the present disclosure.

[0015] FIG. 4A illustrates an example waveform generator, in accordance with certain embodiments of the present disclosure.

[0016] FIG. 4B is a timing diagram showing states of switches of the waveform generator of FIG. 4A.

[0017] FIG. 5 illustrates the IED associated with the waveform shown in FIG. 3, in accordance with certain embodiments of the present disclosure.

[0018] FIG. 6 is a process flow diagram illustrating a method for waveform generation.

DETAILED DESCRIPTION

[0019] Some embodiments of the present disclosure are generally directed to techniques for generating a waveform for controlling ion energy distribution (IED) during plasma processing. For example, a pulsed voltage waveform may be generated by time multiplexing voltage pulses from different sources (e.g., switches) and applied to one or more electrodes in a plasma processing chamber for plasma processing. In some embodiments, the pulsed voltage waveform may be generated using multiple switch pairs, allowing for the pulsed voltage waveform to have a higher frequency as compared to conventional implementations that use a single switch pair. Due to physical and practical device limitations found in current conventional high voltage switching components, switching speeds for these conventional high voltage switches are limited to a “maximum practical switching speed” due to the heat generated in the components during use. During typical plasma processing processes, high voltage pulsed voltage waveforms that are generated by the high voltage switches typically require the switches to repeatedly perform over the lifetime of the switch containing device at voltage levels greater than about 200 volts, such as greater than about 500 volts, or greater than about 800 volts, or greater than about 1000 volts, or even greater than about 5000 volts. In one example, maximum practical switching speeds for conventional switches, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), are typically limited to about 2.5 microseconds (μs) at switching voltages greater than about 800 volts. However, the use of higher frequency voltage waveforms can reduce the voltage droop during the ion current stage of a voltage pulse used during plasma processing. As a result, a narrower IED may be achieved, facilitating greater precision for plasma processing as described in more detail herein. As used herein, a voltage droop generally refers to an increase in voltage established at an electrode during a negative voltage containing portion of a voltage pulse.

Plasma Processing System Examples

[0020] FIG. 1 is a schematic cross-sectional view of a processing system 10 configured to perform one or more of the plasma processing methods set forth herein. In some embodiments, the processing systems 10 is configured for plasma-assisted etching processes, such as a reactive ion etch (RIE) plasma processing. However, it should be noted that the embodiments described herein may be also be used with processing systems configured for use in other plasma-assisted processes, such as plasma-enhanced deposition processes, for example, plasma-enhanced chemical vapor deposition (PECVD) processes, plasma-enhanced physical vapor deposition (PEPVD) processes, plasma-enhanced atomic layer deposition (PEALD) processes, plasma treatment processing or plasma-based ion implant processing, for example, plasma doping (PLAD) processing.

[0021] As shown, the processing system 10 is configured to form a capacitively coupled plasma (CCP), where the processing chamber 100 includes an upper electrode (e.g., chamber lid 123) disposed in a processing volume 129 facing a lower electrode (e.g., the substrate support assembly 136) also disposed in the processing volume 129. In a typical capacitively coupled plasma (CCP) processing system, a radio frequency (RF) source (e.g., RF generator 118) is electrically coupled to one of the upper or lower electrode, and delivers an RF signal configured to ignite and maintain a plasma (e.g., the plasma 101). In this configuration, the plasma is capacitively coupled to each of the upper and lower electrodes and is disposed in a processing region therebetween. Typically, the opposing one of the upper or lower electrodes is coupled to ground or to a second RF power source. In one embodiment, one or more components of the substrate support assembly 136, such as the support base 107 is electrically coupled to a plasma generator assembly 163, which includes the RF generator 118, and the chamber lid 123 is electrically coupled to ground. As shown, the processing system 10 includes a processing chamber 100, a support assembly 136, and a system controller 126.

[0022] The processing chamber 100 typically includes a chamber body 113 that includes the chamber lid 123, one or more sidewalls 122, and a chamber base 124, which collectively define the processing volume 129. The one or more sidewalls 122 and chamber base 124 generally include materials that are sized and shaped to form the structural support for the elements of the processing chamber 100 and are

configured to withstand the pressures and added energy applied to them while a plasma 101 is generated within a vacuum environment maintained in the processing volume 129 of the processing chamber 100 during processing. In one example, the one or more sidewalls 122 and chamber base 124 are formed from a metal, such as aluminum, an aluminum alloy, or a stainless steel alloy.

[0023] A gas inlet 128 disposed through the chamber lid 123 is used to deliver one or more processing gases to the processing volume 129 from a processing gas source 119 that is in fluid communication therewith. A substrate 103 is loaded into, and removed from, the processing volume 129 through an opening (not shown) in one of the one or more sidewalls 122, which is sealed with a slit valve (not shown) during plasma processing of the substrate 103.

[0024] The system controller 126, also referred to herein as a processing chamber controller, includes a central processing unit (CPU) 133, a memory 134, and support circuits 135. The system controller 126 is used to control the process sequence used to process the substrate 103, including the substrate biasing methods described herein. The CPU 133 is a general-purpose computer processor configured for use in an industrial setting for controlling the processing chamber and sub-processors related thereto. The memory 134 described herein, which is generally non-volatile memory, may include random access memory, read-only memory, floppy or hard disk drive, or other suitable forms of digital storage, local or remote. The support circuits 135 are conventionally coupled to the CPU 133 and comprise cache, clock circuits, input/output subsystems, power supplies, and the like, and combinations thereof. Software instructions (program) and data can be coded and stored within the memory 134 for instructing a processor within the CPU 133. A software program (or computer instructions) readable by CPU 133 in the system controller 126 determines which tasks are performable by the components in the processing system 10.

[0025] Typically, the program, which is readable by CPU 133 in the system controller 126, includes code, which, when executed by the processor (CPU 133), performs tasks relating to the plasma processing schemes described herein. The program may include instructions that are used to control the various hardware and electrical components within the processing system 10 to perform the various process tasks and various process sequences used to implement the methods described herein. In one

embodiment, the program includes instructions that are used to perform one or more of the operations described below in relation to FIG. 6.

[0026] The processing system may include a plasma generator assembly 163, a first pulsed voltage (PV) source assembly 196 for establishing a first PV waveform at a bias electrode 104, and a second PV source assembly 197 for establishing a second PV waveform at an edge control electrode 115. The first PV waveform or the second PV waveform may be generated using a waveform generator as described in more detail herein with respect to FIGs. 3, 4A, and 4B. In some embodiments, the plasma generator assembly 163 delivers an RF signal to the support base 107 (e.g., power electrode or cathode) which may be used to generate (maintain and/or ignite) a plasma 101 in a processing region disposed between the substrate support assembly 136 and the chamber lid 123. In some embodiments, the RF generator 118 is configured to deliver an RF signal having a frequency that is greater than 1 MHz or more, or about 2 MHz or more, such as about 13.56 MHz or more.

[0027] As discussed above, in some embodiments, the plasma generator assembly 163, which includes an RF generator 118 and an RF generator assembly 160, is generally configured to deliver a desired amount of a continuous wave (CW) or pulsed RF power at a desired substantially fixed sinusoidal waveform frequency to a support base 107 of the substrate support assembly 136 based on control signals provided from the system controller 126. During processing, the plasma generator assembly 163 is configured to deliver RF power (e.g., an RF signal) to the support base 107 disposed proximate to the substrate support 105, and within the substrate support assembly 136. The RF power delivered to the support base 107 is configured to ignite and maintain a processing plasma 101 of processing gases disposed within the processing volume 129.

[0028] In some embodiments, the support base 107 is an RF electrode that is electrically coupled to the RF generator 118 via an RF matching circuit 162 and a first filter assembly 161, which are both disposed within the RF generator assembly 160. The first filter assembly 161 includes one or more electrical elements that are configured to substantially prevent a current generated by the output of a PV waveform generator 150 from flowing through an RF power delivery line 167 and damaging the RF generator 118. The first filter assembly 161 acts as a high impedance (e.g., high

Z) to the PV signal generated from a PV pulse generator P1 within the PV waveform generator 150, and thus inhibits the flow of current to the RF matching circuit 162 and RF generator 118.

[0029] In some embodiments, the RF generator assembly 160 and RF generator 118 are used to ignite and maintain a processing plasma 101 using the processing gases disposed in the processing volume 129 and fields generated by the RF power (RF signal) delivered to the support base 107 by the RF generator 118. The processing volume 129 is fluidly coupled to one or more dedicated vacuum pumps through a vacuum outlet 120, which maintain the processing volume 129 at sub-atmospheric pressure conditions and evacuate processing and/or other gases, therefrom. In some embodiments, the substrate support assembly 136, disposed in the processing volume 129, is disposed on a support shaft 138 that is grounded and extends through the chamber base 124. However, in some embodiments, the RF generator assembly 160 is configured to deliver an RF power to the bias electrode 104 disposed in the substrate support 105 versus the support base 107.

[0030] The substrate support assembly 136, as briefly discussed above, generally includes the substrate support 105 (e.g., ESC substrate support) and support base 107. In some embodiments, the substrate support assembly 136 can additionally include an insulator plate 111 and a ground plate 112, as is discussed further below. The support base 107 is electrically isolated from the chamber base 124 by the insulator plate 111, and the ground plate 112 is interposed between the insulator plate 111 and the chamber base 124. The substrate support 105 is thermally coupled to and disposed on the support base 107. In some embodiments, the support base 107 is configured to regulate the temperature of the substrate support 105, and the substrate 103 disposed on the substrate support 105, during substrate processing.

[0031] Typically, the substrate support 105 is formed of a dielectric material, such as a bulk sintered ceramic material, such as a corrosion-resistant metal oxide or metal nitride material, for example, aluminum oxide (Al_2O_3), aluminum nitride (AlN), titanium oxide (TiO), titanium nitride (TiN), yttrium oxide (Y_2O_3), mixtures thereof, or combinations thereof. In embodiments herein, the substrate support 105 further includes the bias electrode 104 embedded in the dielectric material thereof. In some embodiments, one or more characteristics of the RF power used to maintain the

plasma 101 in the processing region over the bias electrode 104 are determined and/or monitored by measuring an RF waveform established at the bias electrode 104.

[0032] In one configuration, the bias electrode 104 is a chucking pole used to secure (i.e., chuck) the substrate 103 to the substrate supporting surface 105A of the substrate support 105 and to bias the substrate 103 with respect to the processing plasma 101 using one or more of the pulsed-voltage biasing schemes described herein. Typically, the bias electrode 104 is formed of one or more electrically conductive parts, such as one or more metal meshes, foils, plates, or combinations thereof.

[0033] In some embodiments, the bias electrode 104 is electrically coupled to a clamping network 116, which provides a chucking voltage thereto, such as static DC voltage between about -5000 V and about 5000 V, using an electrical conductor, such as the coaxial power delivery line 106 (e.g., a coaxial cable). As will be discussed further below, the clamping network 116 includes bias compensation circuit elements 116A, a DC power supply 155, and a bias compensation module blocking capacitor, which is also referred to herein as the blocking capacitor C_5. The blocking capacitor C_5 is disposed between the output of a pulsed voltage (PV) waveform generator 150 and the bias electrode 104.

[0034] The substrate support assembly 136 may further include the edge control electrode 115 that is positioned below the edge ring 114 and surrounds the bias electrode 104 and/or is disposed a distance from a center of the bias electrode 104. In general, for a processing chamber 100 that is configured to process circular substrates, the edge control electrode 115 is annular in shape, is made from a conductive material, and is configured to surround at least a portion of the bias electrode 104. In some embodiments, such as shown in FIG. 1, the edge control electrode 115 is positioned within a region of the substrate support 105. In some embodiments, as illustrated in FIG. 1, the edge control electrode 115 includes a conductive mesh, foil, and/or plate that is disposed a similar distance (i.e., Z-direction) from the substrate supporting surface 105A of the substrate support 105 as the bias electrode 104. In some other embodiments, the edge control electrode 115 includes a conductive mesh, foil, and/or plate that is positioned on or within a region of a quartz pipe 110, which surrounds at least a portion of the bias electrode 104 and/or the

substrate support 105. Alternately, in some other embodiments (not shown), the edge control electrode 115 is positioned within or is coupled to the edge ring 114, which is disposed on and adjacent to the substrate support 105. In this configuration, the edge ring 114 is formed from a semiconductor or dielectric material (e.g., AlN, etc.).

[0035] The edge control electrode 115 can be biased by use of a PV waveform generator that is different from the PV waveform generator 150 that is used to bias the bias electrode 104. In some embodiments, the edge control electrode 115 can be biased by use of a PV waveform generator 150 that is also used to bias the bias electrode 104 by splitting part of the power to the edge control electrode 115. In one configuration, a first PV waveform generator 150 of the first PV source assembly 196 is configured to bias the bias electrode 104, and a second PV waveform generator 150 of a second PV source assembly 197 is configured to bias the edge control electrode 115.

[0036] A power delivery line 157 electrically connects the output of the PV waveform generator 150 of the first PV source assembly 196 to an optional filter assembly 151 and the bias electrode 104. While the discussion below primarily discusses the power delivery line 157 of the first PV source assembly 196, which is used to couple a PV waveform generator 150 to the bias electrode 104, the power delivery line 158 of the second PV source assembly 197, which couples a PV waveform generator 150 to the edge control electrode 115, will include the same or similar components. The electrical conductor(s) within the various parts of the power delivery line 157 may include: (a) one or a combination of coaxial cables, such as a flexible coaxial cable that is connected in series with a rigid coaxial cable, (b) an insulated high-voltage corona-resistant hookup wire, (c) a bare wire, (d) a metal rod, (e) an electrical connector, or (f) any combination of electrical elements in (a) – (e). The optional filter assembly 151 includes one or more electrical elements that are configured to substantially prevent a current generated by the output of the RF generator 118 from flowing through the power delivery line 157 and damaging the PV waveform generator 150. The optional filter assembly 151 acts as a high impedance (e.g., high Z) to RF signal generated by the RF generator 118, and thus inhibits the flow of current to the PV waveform generator 150.

[0037] The second PV source assembly 197 includes a clamping network 116 so that a bias applied to the edge control electrode 115 can be similarly configured to the bias applied to the bias electrode 104 by the clamping network 116 coupled within the first PV source assembly 196. Applying similarly configured PV waveforms and clamping voltages to the bias electrode 104 and edge control electrode 115 can help improve the plasma uniformity across the surface of the substrate during processing and thus improve the plasma processing process results.

[0038] In some embodiments, the processing chamber 100 further includes the quartz pipe 110, or collar, that at least partially circumscribes portions of the substrate support assembly 136 to prevent the substrate support 105 and/or the support base 107 from contact with corrosive processing gases or plasma, cleaning gases or plasma, or byproducts thereof. Typically, the quartz pipe 110, the insulator plate 111, and the ground plate 112 are circumscribed by a liner 108. In some embodiments, a plasma screen 109 is positioned between the cathode liner 108 and the sidewalls 122 to prevent plasma from forming in a volume underneath the plasma screen 109 between the liner 108 and the one or more sidewalls 122.

[0039] FIG. 2A illustrates an example voltage waveform 200 established at a substrate in a processing chamber (e.g., processing chamber 100). In this example, the waveform 200 is generated due to the application of a waveform by the PV waveform generator 150 of the first PV source assembly 196. The waveform 200 includes an ion current stage and a sheath collapse stage, as shown. At the beginning of the ion current stage, a drop of substrate voltage, which is created by the falling edge 204, creates a high voltage sheath to form above the substrate, accelerating positive ions to the substrate. The positive ions that bombard the surface of the substrate during the ion current stage deposit a positive charge on the substrate surface, which, if uncompensated, causes a gradual increase of the substrate voltage positively (i.e., positive slope during phase 205 of the voltage waveform 200) during the ion current stage, as shown. However, the uncontrolled accumulation of positive charge on the substrate surface undesirably gradually discharges the sheath and chuck capacitors, slowly decreasing the sheath voltage drop and bringing the substrate potential closer to zero. The accumulation of positive charge results in the

voltage droop (i.e., positive slope during phase 205) in the voltage waveform established at the substrate.

[0040] The voltage difference between the beginning and end of the ion current phase determines an ion energy distribution function (IEDF) width. FIG. 2B illustrates the effect of increasing plasma density, on a voltage waveform that is established on a substrate by use of a PV source, such as a waveform generator 150. As shown, an increase in plasma density during plasma processing (i.e., arrow highlights direction), due to changes in one or more plasma processing parameters (e.g., RF power applied by the plasma generator assembly 163), will tend to increase the voltage difference from the start to the end of the ion current stage, and thus undesirably increase the voltage droop. The greater the voltage difference, the wider the IEDF width. For example, as shown in FIG. 2C, the ion energy distribution (IED) 201 broadens with increasing ion current variation without compensation for the substrate's voltage rise. Therefore, by use of the higher frequency voltage waveforms techniques disclosed herein, the voltage droop in the voltage waveforms created by increasing plasma density during plasma processing can be reduced, which results in a narrower IED, and thus greater precision in the on-substrate plasma processing results.

[0041] In the reactor, plasma may be generated by an inductively coupled source on top of the substrate (or a peripheral coil). The coil may be placed on top of a ceramic lid (vacuum boundary), or by applying RF power to either the electrostatic chuck or a top electrode in the case of capacitively coupled plasma reactors. As described, the waveform generator (e.g., waveform generator 150 of the first PV source assembly 196) outputs a bipolar and short narrow positive pulse that transitions from a negative voltage to a positive voltage greater than zero, as shown in FIG. 2A. The duration of the positive voltage pulse is controlled and transitions back to the negative voltage baseline. The voltage stays negative and transitions back to a positive pulse at the end of the period labeled T_{ON}. The transition back to the positive pulse is completed during the rising edge 202 portion of the voltage waveform 200. The duration of the positive section of the pulse can be varied, and, in some embodiments, is between 1% and 20% of the waveform period (T_p), such as between 5% and 15% of the waveform period (T_p). In one example, the waveform period may be about 5 µs and the frequency of the waveform 200 may be about 200kHz. In

another example, the waveform period may be about 2.5 μs and the frequency of the waveform 200 is about 400kHz.

[0042] During a portion of the voltage waveform, plasma bulk electrons are attracted to the substrate surface due to the rising edge 202 of the pulse step, but those electrons cannot establish a negative DC sheath potential yet as there are equal amounts of positive charge on the electrode (e.g., electrode 104). The substrate and the dielectric disposed between the electrode and the substrate supporting surface 105A form a capacitor, which has an effective capacitance C_{esc}, which will allow an equal amount of positive charge on the electrode to cancel the field generated by the electrons disposed on the substrate surface. At the falling edge 204 of the pulse step, the positive charge on the electrode is neutralized by the electrons from the waveform generator, and therefore, a negative DC voltage is established on the substrate surface. If the formed DC voltage is held constant, then mono-energy ion bombardment is achieved. The negative DC voltage (Vdc) can be approximated by using the magnitude of the falling edge (ΔV) and the ratio between the C_{esc} and the sheath capacitance C_{sheath} in accordance with the following equation:

$$Vdc = \Delta V * C_{esc}/(C_{esc} + C_{sheath})$$

Generation Technique for Waveform Generation

[0043] As semiconductor device features shrink, atomic precision is often required during today's substrate processing techniques, such as plasma etching and plasma deposition techniques. For etching processes where the plasma ions play a major role, precise ion energy control is often required. Traditionally radio frequency (RF) biased approaches use a sinusoidal wave to excite plasma and accelerate ions. The ion energy distribution (IED) from conventional RF technology is typically of bimodal shape. Pulsing techniques have also been explored in recent years to generate IEDs with a mono-energy peak.

[0044] In some implementations, due to system complexity and equipment cost related issues, positive ion current is not compensated for during the ion current stage of the voltage waveform, and therefore, the negative voltage on the substrate decays with time (e.g., becoming less negative). In other words, as described with respect to waveform 200, without compensation, the substrate voltage rises during the ion

current stage, also referred to herein as a voltage droop. This trend gets worse with increasing plasma density (e.g., increasing ion current), which cause the IED to expand or broaden towards the lower energy regime, as shown in FIG. 2C.

[0045] In some cases, a ramp voltage is generated to compensate for this voltage rise during portions of the ion current stage (e.g., at least during phase 205), by use of a current source or a plurality of voltage sources that are coupled to the electrode (e.g., electrode 104). However, at higher voltages (e.g., greater than 5kV), it is challenging to generate custom-tailored waveforms with a ramp to compensate for this voltage rise.

[0046] In some embodiments, a high frequency voltage waveform may be used to lessen the impact of this voltage rise (i.e., droop) created during the ion current stage. With the current state of high voltage switches that are available on the market today, generating high frequency voltage pulse trains at pulse repetition frequency greater than 400 kHz is problematic, due to physical and practical device limitations found in these conventional components. Therefore, as briefly discussed above, switching speeds for these conventional high voltage switches are limited to a maximum practical switching speed due to damage created in these components at moderate to high frequencies due to heat generated during use. In certain embodiments of the present disclosure, time-domain multiplexing of voltage pulses is used to generate a waveform to be provided to a complex load (e.g., the electrostatic chuck and plasma 101 (FIG. 1) such that the load receives pulses at a higher frequency, mitigating the effects of the voltage droop at the substrate surface. For example, positive voltage pulses at a frequency of around 400kHz may be used to periodically establish a negative direct current (DC) bias on the substrate, thereby obtaining IEDs with a mono-energy peak. In other words, by the time the voltage at the substrate surface voltage rises to a specific threshold during the ion current stage of a first voltage waveform pulse, a second voltage waveform pulse (e.g., from a different source or switches) may be applied, in effect resetting the voltage at the substrate surface during a following pulse cycle, as described in more detail herein.

[0047] FIG. 3 illustrates a pulsed voltage-biasing scheme using a waveform 300, in accordance with certain embodiments of the present disclosure. As shown, a first pulsed voltage cycle 320 and a second pulsed voltage cycle 322 may be time-

multiplexed. To the electrostatic chuck and plasma 101, it appears that the frequency of the voltage pulse has increased due to the interleaving of the first pulsed voltage cycle 320 and the second pulsed voltage cycle 322. As the substrate voltage begins drooping during the ion current stage of the first voltage cycle, which is generated from a first PV source, a second pulse is generated by a second PV source, is applied, restoring the DC voltage bias (negative) on the substrate and restoring the falling ion energy caused by the droop.

[0048] In other words, the waveform 300 may include a positive voltage pulse 302 and a negative voltage pulse 304 for the first pulsed voltage cycle 320, followed by another positive voltage pulse 306 and another negative voltage pulse 308 for the second pulsed voltage cycle 322, as shown in FIG. 3. In some embodiments, the positive voltage pulse 302 and negative voltage pulse 304 may be generated using a switch pair (e.g., S1 and S3 in FIG. 4A), and the other positive voltage pulse 306 and other negative voltage pulse 308 may be generated using another switch pair (e.g., S2 and S4 in FIG. 4A). Using the different switch pairs allows for a higher frequency waveform as compared to conventional implementations where only a single switch pair is used for generation of positive and negative pulses. In other words, each switch may be implemented using one or more transistors, such as metal oxide semiconductor field-effect transistors (MOSFETs). Due to heating, each of the MOSFETs may have a switching frequency limit (e.g., maximum practical switching speed), preventing a single switch pair from generating pulses at a high frequency (e.g., 400kHz). If a switch is operating at a frequency that is greater than the switching frequency limit of the switch, the voltage drop across the switch may increase due to an increase in the switch resistance resultant from the heat generated in the switch due to the presence of the high switching voltage. For example, the voltage drop across the switch may increase by 10% or more, depending on the switching frequency and type of switch. Moreover, if multiple switches are coupled in series, the drop across the switches accumulate. In other words, if three switches are coupled to in series (e.g., to implement switch S1, S2, S3, or S4), and the voltage drop across each switch increases by 10%, then the total voltage drop across the switches may increase by 30%. It is also believed that voltage drops across a switch that are ≥10% when comparing the voltage drop across a switch at a switch's switching frequency limit versus a time when the switch is initially placed into use, at the same switch input

voltage, can lead to permanent damage to the components within the switch (e.g., increased switching resistance overtime) and/or significantly shorter than normal switch lifetimes.

[0049] FIG. 4A illustrates a waveform generator 400 for generating the pulses during the first and second pulsed voltage cycles 320, 322, in accordance with certain embodiments of the present disclosure. The waveform generator 400 may be part of the PV waveform generator 150. FIG. 4B is a timing diagram 401 showing the state of switches of the waveform generator 400.

[0050] As shown, switch S1 may be closed during a phase, coupling the waveform generator output node 402 to a voltage source V1 of the voltage source circuitry 410 and generating the positive voltage pulse 302. The switch S1 is then opened, and switch S3 is closed during a second phase, grounding the output node 402. Grounding the output node 402 results in the negative voltage pulse 304. In other words, during the positive voltage pulse 302, a capacitance between the output node 402 and the substrate charges. After the positive voltage pulse 302, the output node 402 is coupled to an electric ground node. Since the voltage across the capacitance between the output node 402 and the substrate cannot change instantaneously, the substrate voltage drops to a negative voltage in response to closure of switch S3.

[0051] After switch S3 is opened, switch S2 is closed during a third phase, coupling the voltage source V2 of the voltage source circuitry 410 to output node 404, in effect implementing the positive voltage pulse 306. Switch S2 is then opened, and switch S4 is closed during a fourth phase, coupling the output node 404 to the electrical ground node to implement the negative voltage pulse 308. The first, second, third, and fourth phases are non-overlapping phases, as shown by timing diagram 401. As shown, the phases may be repeated to generate a continuous time-multiplexed pulsed waveform that is delivered at a frequency that is greater than the maximum practical switching speed of each individual switch. In one example, if the maximum practical switching speed limit of each switch limits the switching frequency of each switch to a frequency of 400 kHz, a two voltage source configuration containing the same switches could deliver a time-multiplexed pulse train that has a frequency greater than 400 kHz and less than or equal to 800 kHz. In one non-limiting example, if the waveform generator 400 is asked to generate an 800 kHz pulse train, the switch

combinations S1/S3 and S2/S4 are each separately used to provide the first and the second pulsed voltage cycles 320, 322, respectively, that will each have a period (T_p) that is 1.25 µs long, but are spaced 2.5 µs apart and staggered in time to form the desired pulse train.

[0052] In some embodiments, the output nodes 402, 404 may be coupled to the same node in the chamber. For example, the output nodes 402, 404 may be coupled to electrode 104. In some embodiments, the output nodes 402, 404 may be coupled to different nodes in the chamber. For example, the output node 402 may be coupled to electrode 104 and the output node 404 may be coupled to electrode 115.

[0053] In some embodiments, a first voltage source circuitry 410 of a waveform generator 400 forms part of the PV waveform generator 150 (FIG. 1) of the first PV source assembly 196. In another embodiment, a first voltage source circuitry 410 of a waveform generator 400 forms part of the PV waveform generator 150 of the first PV source assembly 196, and a second voltage source circuitry 410 of a waveform generator 400 forms part of the PV waveform generator 150 of the second PV source assembly 197. In yet another embodiment, a first voltage source circuitry 410 of a waveform generator 400 forms part of the PV waveform generator 150 of the first PV source assembly 196, a second voltage source circuitry 410 of a waveform generator 400 forms part of the PV waveform generator 150 of the second PV source assembly 197, and/or a third voltage source circuitry 410 of a waveform generator 400 forms part of the PV waveform generator 150 of a third PV source assembly 198 that is coupled to the lid 123. In either of these configurations, and where appropriate, the output nodes 402, 404 of the first voltage source circuitry 410 are coupled to electrode 104, the output nodes 402, 404 of the second voltage source circuitry 410 are coupled to electrode 115, and/or the output nodes 402, 404 of the third voltage source circuitry 410 are coupled to lid 123.

[0054] In some embodiments, the voltage source circuitry 410 may include a first voltage source V1 coupled to the switch S1 and a second voltage source V2 coupled to the switch S2. Each of the first and second voltage sources may be implemented using a capacitive element that is charged to a specific voltage by a power source. In some embodiments, the first and second voltage sources V1 or V2 of each voltage source circuitry 410 may provide different voltages or the same voltage.

[0055] While the examples provided herein have described two switch pairs to facilitate understanding, the embodiments of the present disclosure may be implemented with more than two switch pairs. For example, in addition to the first switch pair (e.g., S1 and S3) and the second switch pair (e.g., S2 and S4), a third switch pair may be implemented for generating positive and negative pulses, allowing for a higher frequency of operation. In other words, after switch S2 and switch S4 are used to generate the positive voltage pulse 306, and negative voltage pulse 308, the third switch pair may be used to generate another positive pulse and another negative pulse before the switch S1 and switch S3 are used to generate the positive voltage pulse 302, and negative voltage pulse 304 again. Thus, in some embodiments, a plurality of switch pairs are utilized in a serial and repeating cycle to form a pulse train that has a frequency that is greater than the maximum practical switching speed of each individual switch, such that the maximum frequency of the pulse train is equal to N times the maximum frequency of each switch or at least the slowest switch of the plurality of switches, where N is equal to the number of switch pairs of the plurality of switch pairs. Operating each of the switch pairs during different phases of the generated pulse train allows for the implementation of a high frequency waveform for plasma processing. Using a higher frequency waveform allows for the voltage droop (e.g., increasing voltage during the ion current stage) to be reduced, increasing plasma processing precision.

[0056] FIG. 5 illustrates the ion energy distribution (IED) associated with the waveform 300, in accordance with certain embodiments of the present disclosure. As shown, when generating the waveform at a higher frequency (e.g., 400 kHz), a narrower IED may be obtained as compared to a lower frequency waveform (e.g., waveform 200 of FIG. 2A having a frequency of 200 kHz). The narrower IED facilitates a greater feature formation precision, for example, during typical etching plasma processes.

[0057] FIG. 6 is a process flow diagram illustrating a method 600 for waveform generation. The method 600 may be performed by a waveform generation system including a waveform generator, such as the waveform generator 400, and a system controller such as the system controller 126.

[0058] The method 600 begin, at activity 602, with the waveform generation system coupling, via a first switch (e.g., switch S1), voltage source circuitry (e.g., voltage source circuitry 410) to a first output node (e.g., output node 402) of a waveform generator (e.g., waveform generator 400), the first output node being coupled to a chamber (e.g., chamber 100). At activity 604, the waveform generation system couples, via a second switch (e.g., switch S3), the first output node to an electrical ground node. At activity 606, the waveform generation system couples, via a third switch (e.g., switch S2), the voltage circuitry to a second output node (e.g. output node 404) of the waveform generator, the second output node being coupled to the chamber. At activity 608, the waveform generation system couples, via a fourth switch (e.g., switch S4), the second output node to the electrical ground node. In some embodiments, the activities 602, 604, 606, 608 may be repeated to generate a waveform for plasma processing.

[0059] In some embodiments, a first pulsed voltage waveform (e.g., including the positive voltage pulse 302 and the negative voltage pulse 304) is generated at the chamber by the coupling via the first switch and the second switch. Moreover, a second pulsed voltage waveform (e.g., including the positive voltage pulse 306 and the negative voltage pulse 308) is generated at the chamber by the coupling via the third switch and the fourth switch. The first pulsed voltage waveform may be phase shifted (e.g., by 180º) from the second pulsed voltage waveform.

[0060] In some embodiments, the coupling via the first switch, the second switch, the third switch, and the fourth switch is during non-overlapping phases. For example, the voltage source circuitry is coupled to the first output node during a first phase of the non-overlapping phases, and the first output node is coupled to the electrical ground node during a second phase of the non-overlapping phases, the second phase being after the first phase. Moreover, the voltage source circuitry is coupled to the second output node during a third phase of the non-overlapping phases, the third phase being after the second phase, and the second output node is coupled to the electrical ground node during a fourth phase of the non-overlapping phases, the fourth phase being after the third phase.

[0061] In some embodiments, the voltage source circuitry includes a first voltage source (e.g., voltage source V1) coupled to the first switch and a second voltage

source (e.g., voltage source V2) coupled to the second switch. The first voltage source may include a first capacitive element, and the second voltage source may include a second capacitive element. Each of the first switch, the second switch, the third switch, and the fourth switch may include one or more transistors (e.g., MOSFETs).

[0062] In some embodiments, the waveform generation system may generate a first positive voltage pulse (e.g., positive voltage pulse 302) at a node (e.g., at a substrate) in the chamber by coupling the voltage source circuitry to the first output node, and generate a first negative voltage pulse (e.g., negative voltage pulse 304) at the node in the chamber by coupling the first output node to the electrical ground node. Moreover, the waveform generation system may generate a second positive voltage pulse (e.g., positive voltage pulse 306) at the node in the chamber by coupling the voltage source circuitry to the second output node, and generate the second negative voltage pulse (e.g., negative voltage pulse 308) at the node in the chamber by coupling the second output node to the electrical ground node.

[0063] The term “coupled” is used herein to refer to the direct or indirect coupling between two objects. For example, if object A physically touches object B and object B touches object C, then objects A and C may still be considered coupled to one another—even if objects A and C do not directly physically touch each other. For instance, a first object may be coupled to a second object even though the first object is never directly physically in contact with the second object.

[0064] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims

1. A plasma processing system comprising:

a voltage waveform generator configured to deliver a voltage waveform to an electrode disposed within a chamber of the plasma processing system, the voltage waveform generator comprising:

voltage source circuitry;

a first switch coupled between the voltage source circuitry and a first output node of the waveform generator, the first output node being configured to be coupled to the electrode;

a second switch coupled between the first output node and electrical ground node;

a third switch coupled between the voltage source circuitry and a second output node of the waveform generator, the second output node being configured to be coupled to the electrode; and

a fourth switch coupled between the second output node and the electrical ground node.

2. The plasma processing system of claim 1, wherein:

the first switch and the second switch are configured to generate a first pulsed voltage waveform to be provided to the electrode; and

the third switch and the fourth switch are configured to generate a second pulsed voltage waveform to be provided to the electrode, the first pulsed voltage waveform being phase shifted from the second pulsed voltage waveform.

3. The plasma processing system of claim 1, wherein the first switch, the second switch, the third switch, and the fourth switch are configured to be closed during non-overlapping phases.

4. The plasma processing system of claim 3, wherein:

the first switch is configured to be closed during a first phase of the non-overlapping phases;

the second switch is configured to be closed during a second phase of the non-overlapping phases, the second phase being after the first phase;

the third switch is configured to be closed during a third phase of the non-overlapping phases, the third phase being after the second phase; and

the fourth switch is configured to be closed during a fourth phase of the non-overlapping phases, the fourth phase being after the third phase.

5. The plasma processing system of claim 1, wherein the voltage source circuitry comprises a first voltage source coupled to the first switch and a second voltage source coupled to the second switch.

6. The plasma processing system of claim 5, wherein the first voltage source comprises a first capacitive element, and wherein the second voltage source comprises a second capacitive element.

7. The plasma processing system of claim 1, wherein each of the first switch, the second switch, the third switch, and the fourth switch comprises one or more transistors.

8. The plasma processing system of claim 1, wherein the first output node is coupled to the second output node.

9. The plasma processing system of claim 1, wherein the electrode is disposed below a substrate supporting surface of a substrate support disposed within the chamber.

10. The plasma processing system of claim 9, wherein at least one of the first switch, the second switch, the third switch, or the fourth switch has a switching frequency limit, and wherein the waveform generator is configured to generate a waveform at the electrode having a frequency that is greater than the switching frequency limit.

11. An apparatus for generating a plasma, comprising:

a processing chamber

a voltage waveform generator configured to deliver a voltage waveform to an electrode disposed within the processing chamber, the voltage waveform generator comprising:

voltage source circuitry; and

one or more switches coupled to the voltage source circuitry, wherein the one or more switches include:

a first switch coupled between the voltage source circuitry and a first output node of the waveform generator, the first output node being configured to be coupled to the electrode;

a second switch coupled between the first output node and electrical ground node;

a third switch coupled between the voltage source circuitry and a second output node of the waveform generator, the second output node being configured to be coupled to the electrode; and

a fourth switch coupled between the second output node and the electrical ground node, and

a system controller configured to control the one or more switches.

12. The apparatus of claim 11, wherein the system controller is configured to close the first switch, the second switch, the third switch, and the fourth switch during non-overlapping phases.

13. The apparatus of claim 12, wherein the system controller is configured to:

close the first switch during a first phase of the non-overlapping phases;

close the second switch during a second phase of the non-overlapping phases, the second phase being after the first phase;

close the third switch during a third phase of the non-overlapping phases, the third phase being after the second phase; and

close the fourth switch during a fourth phase of the non-overlapping phases, the fourth phase being after the third phase.

14. The apparatus of claim 11, wherein the voltage source circuitry comprises a first voltage source coupled to the first switch and a second voltage source coupled to the third switch.

15. The apparatus of claim 11, wherein the electrode is disposed below a substrate supporting surface of a substrate support disposed within the processing chamber.

16. The apparatus of claim 15, wherein at least one of the first switch, the second switch, the third switch, or the fourth switch has a switching frequency limit, and wherein the apparatus is configured to generate a waveform at the electrode having a frequency that is greater than the switching frequency limit.

17. A plasma processing system comprising:

a voltage waveform generator configured to deliver a voltage waveform to a chamber of the plasma processing system, the voltage waveform generator comprising:

a first voltage source circuitry included in a first pulsed waveform (PV) source assembly;

a second voltage source circuitry included in a second PV source assembly;

a first pair of switches coupled to the first voltage source circuitry comprising a first switch coupled between the first voltage source circuity and a first output node configured to be coupled to the chamber and a second switch coupled between the first output node and electrical ground node; and

a second pair of switches coupled to the first voltage source circuitry comprising a third switch coupled between the first voltage source circuity and a second output node configured to be coupled to the chamber and a fourth switch coupled between the second output node and electrical ground node;

a third pair of switches coupled to the second voltage source circuitry comprising a fifth switch coupled between the second voltage source circuity and a third output node configured to be coupled to the chamber and a sixth switch coupled between the third output node and electrical ground node;

a fourth pair of switches coupled to the second voltage source circuitry comprising a seventh switch coupled between the second voltage source circuity and a fourth output node configured to be coupled to the chamber and an eighth switch coupled between the fourth output node and electrical ground node.

18. The plasma processing system of claim 17, wherein

the first output node and the second output node are coupled to a first electrode disposed within the chamber, and the third output node and the fourth output node are coupled to a second electrode disposed within the chamber.

19. The plasma processing system of claim 18, further comprising:

a third voltage source circuitry;

a ninth switch coupled between the third voltage source circuitry and a fifth output node of the waveform generator, the fifth output node being configured to be coupled to the chamber;

a tenth switch coupled between the fifth output node and electrical ground node;

an eleventh switch coupled between the third voltage source circuitry and a sixth output node of the waveform generator, the sixth output node being configured to be coupled the chamber; and

a twelfth switch coupled between the sixth output node and electrical ground node.

20. The plasma processing system of claim 19, the fifth output node and the sixth output node are coupled a lid of the chamber.