CLAIMS

What is claimed is:

1. A semiconductor device package (10) comprising:

a semiconductor device (12) including a substrate (14) composed of a semiconductor material and a plurality of metallic connection pads (16) formed on the substrate (14), the plurality of metallic connection pads (16) being formed on each of first and second opposing surfaces (18, 20) of the semiconductor device (12) with edges (24) of the semiconductor device (12) extending between the first and second surfaces (18, 20);

a first passivation layer (22) applied on the semiconductor device (12), the first passivation layer (22) being applied so as to cover the semiconductor device (12) including the plurality of metallic connection pads (16) formed on the substrate (14);

a base dielectric laminate sheet (42) affixed to the first surface (18) of the semiconductor device (12), the base dielectric laminate sheet (42) having a thickness greater than that of the first passivation layer (22);

a second passivation layer (30) applied over the first passivation layer (22) and the semiconductor device (12) and having a thickness greater than that of the first passivation layer (22), with the second passivation layer (30) covering the second surface (20) and the edges (24) of the semiconductor device (12); and

a plurality of metal interconnects (36) electrically coupled to the plurality of metallic connection pads (16) of the semiconductor device (12), each of the plurality of metal interconnects (36) extending through a respective via (34) formed through the first and second passivation layers (18, 20) and the base dielectric laminate sheet (42) to form a direct metallic connection with one of the plurality of metallic connection pads (16).

2. The semiconductor device package (10) of claim 1 wherein the first passivation layer (22) comprises one of silicon nitride and silicon oxide.

3. The semiconductor device package (10) of claim 1 wherein the second passivation layer (30) comprises at least one dielectric laminate sheet applied over the first passivation layer (22) and the second surface and edges (24) of the semiconductor device (12), with the at least one dielectric laminate sheet being formed to substantially match a shape of the semiconductor device (12).

4. The semiconductor device package (10) of claim 3 further comprising an adhesive layer positioned between the first passivation layer (22) and the second passivation layer (30).

5. The semiconductor device package (10) of claim 1 wherein the second passivation layer (30) comprises a liquid dielectric material applied over the first passivation layer (22) and the second surface (20) and edges (24) of the semiconductor device (12) so as to substantially match a shape of the semiconductor device (12), the liquid dielectric material being applied via one of a spray application, a molding application, and a selective deposition application.

6. The semiconductor device package (10) of claim 1 further comprising an additional dielectric laminate sheet (74) affixed to the base dielectric laminate sheet (42) and extending out past a perimeter of the semiconductor device (12).

7. The semiconductor device package (10) of claim 6 wherein the plurality of metal interconnects (36) extends out past the perimeter of the semiconductor device (12) and onto the additional dielectric laminate sheet (74).

8. The semiconductor device package (10) of claim 6 further comprising a lap joint (90) formed on the additional dielectric laminate sheet (74) extending out past the perimeter of the semiconductor device (12), wherein the lap joint (90) is configured to couple the semiconductor device package (10) with another semiconductor device package (94).

9. The semiconductor device package (10) of claim 1 wherein the semiconductor device (12) comprises an optical diode, with the semiconductor device package (10) further comprising an optical window (82) formed through one of the base dielectric laminate sheet (42) and the second passivation layer (30) so as to expose one surface of the optical diode.

10. The semiconductor device package (10) of claim 1 wherein the second passivation layer (30) is configured to have a thickness that provides a desired breakdown voltage for the semiconductor device package (10) and that also provides a minimized parasitic inductance for the semiconductor device package (10).

CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device package comprising:

a semiconductor device including a substrate composed of a semiconductor material and a plurality of metallic connection pads formed on the substrate, the plurality of metallic connection pads being formed on each of first and second opposing surfaces of the substrate with edges of the semiconductor device extending between the first and second surfaces;

a first passivation layer applied on the semiconductor device, the first passivation layer being applied so as to cover the semiconductor device including the plurality of metallic connection pads formed on the substrate;

a base dielectric laminate sheet affixed to the first surface of the semiconductor device, the base dielectric laminate sheet having a thickness greater than that of the first passivation layer;

a second passivation layer applied over the first passivation layer and the semiconductor device and having a thickness greater than that of the first passivation layer, with the second passivation layer covering the second surface and the edges of the semiconductor device; and

a plurality of metal interconnects electrically coupled to the plurality of metallic connection pads of the semiconductor device, each of the plurality of metal interconnects extending through a respective via formed through the first and second passivation layers or through the base dielectric laminate sheet to form a direct metallic connection with one of the plurality of metallic connection pads.

2. The semiconductor device package of claim 1 wherein the first passivation layer comprises one of silicon nitride and silicon oxide.

3. The semiconductor device package of claim 1 wherein the second passivation layer comprises at least one dielectric laminate sheet applied over the first passivation layer and the second surface and edges of the semiconductor device, with the at least one dielectric laminate sheet being formed to substantially match a shape of the semiconductor device.

4. The semiconductor device package of claim 3 further comprising an adhesive layer positioned between the first passivation layer and the second passivation layer.

5. The semiconductor device package of claim 1 wherein the second passivation layer comprises a liquid dielectric material applied over the first passivation layer and the second surface and edges of the semiconductor device semiconductor device so as to substantially match a shape of the semiconductor device, the liquid dielectric material being applied via one of a spray application, a molding application, and a selective deposition application.

6. The semiconductor device package of claim 1 further comprising an additional dielectric laminate sheet affixed to the base dielectric laminate sheet semiconductor device and extending out past a perimeter of the semiconductor device.

7. The semiconductor device package of claim 6 wherein the plurality of metal interconnects extends out past the perimeter of the semiconductor device and onto the additional dielectric laminate sheet.

8. The semiconductor device package of claim 6 further comprising a lap joint formed on the additional dielectric laminate sheet extending out past the perimeter of the semiconductor device, wherein the lap joint is configured to couple the semiconductor device package with another semiconductor device package.

9. The semiconductor device package of claim 1 wherein the semiconductor device comprises an optical diode.

10. The semiconductor device package of claim 9 further comprising an optical window formed through one of the base dielectric laminate sheet and the second passivation layer so as to expose one surface of the optical diode.

11. The semiconductor device package of claim 1 wherein the second passivation layer is configured to have a thickness that provides a desired breakdown voltage for the semiconductor device package and that also provides a minimized parasitic inductance for the semiconductor device package.