PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Junction Transistor

We, TEXAS INSTRUMENTS INCORPORATED, of 6000, Lemmon Avenue, Dallas, Texas, United States of America, a Corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a transistor arrangement and more particularly to an improved method for making it.

The performance of junction transistors manufactured using conventional techniques of assembly is quite often limited by the dimensions of the base region, the method of forming an electrical connection between the base region and the lead wire and the location of this connection in the base region. This is true whether the transistor is a grown junction, alloyed junction, diffused junction, or other type. It will be recalled that it is accepted practice to connect the base lead of a grown junction transistor to the exposed peripheral edge of the base region. Base lead connections to alloyed junction or diffused junction transistors are usually made to an exposed surface of the material forming the base region at a point slightly removed from the junction area. In all base lead connections the conductivity of the material of the base region is relied on to carry the modulating signal to all portions of the base region. Unfortunately, however, the resistance of semiconductor material to current flow is quite high and base lead connections of the type described above produce unequal current distribution through the base layer. For improved performance, it is desirable to have the current densities of all parts of the base layer as nearly equal as possible.

It is an object of the present invention to provide a method of making a junction transistor in which improved base region current distribution is achieved through an improved base lead connection arrangement without sacrificing other performance characteristics.

It is a still further object of the present invention to provide a method for making an improved transistor of the junction type exhibiting superior performance over conventional junction transistors more particularly as regards increased breakdown voltage.

In a method of making a junction type transistor comprising two outer layers of the same conductivity type with an intermediate base layer of intermediate conductivity type therebetween, according to the invention an electrical connection is made to said base layer by the steps of providing in one outer layer an alloying zone which is joined to the base layer and which has a small but appreciable thickness, and alloying through said alloying zone a lead wire comprised of a material which produces the same conductivity type as said base layer to form the required electrical connection.

Preferably said alloying zone comprises a recess in one of said outer layers, with the bottom of the recess being spaced by a small but appreciable thickness from the intermediate base layer of the transistor.

The invention is illustrated by way of example in the accompanying diagrammatic drawings, in which:

Fig. 1 is a view in end elevation of a junction transistor made according to the present invention;

Fig. 2 is a view in section taken on the plane parallel with the end viewed in Fig. 1 illustrating the first step in the method;

Fig. 3 is a view in section similar to Fig. 2 demonstrating the manner of making connection to the base region;

Fig. 4 is a view in section similar to Fig. 3 illustrating the manner in which a plurality of connections may be made; and

Fig. 5 is a view in section through a thin wafer illustrating the manner of making connection through an outer layer.

Referring now to the drawing, there will

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be described the preferred embodiment of the present invention. As will be evident from Fig. 1, there is illustrated in end elevation a junction type transistor which consists of outer layers 10 and 11 with a relatively thin intermediate layer 12. The block itself is composed of a semiconductor material which may be either silicon or germanium. The material of the two outer layers 10 and 11 is characterized by one type of conductivity, either n or p and the material of the thin intermediate layer 12 is characterized by the opposite type of conductivity. Thus, it will be understood that the transistor block illustrated may be either an n-p-n or a p-n-p block but, for purposes of illustration, it will be considered to be an n-p-n type.

The block may be of any junction type such as for example grown junction, alloyed junction, or diffused junction. If of the grown junction type, it is produced by the usual method of growing a single crystal of semiconductor material in a conventional crystal puller and introducing into the melt, at succeeding stages of the crystal growth, impurities to produce regions of a desired conductivity type in the crystal. As is well-known, n-type conductivity semiconductor material is produced by any one or a combination of impurities such as arsenic, bismuth, antimony, phosphorus and others. P-type conductivity is produced by impurities such as aluminium, boron, gallium, thallium, indium and others. After the crystal has been grown, it is cut up into a plurality of segments like the wafer illustrated in Fig. 1. Such a grown junction transistor block may also be cut from a crystal in which regions of alternating conductivity type have been produced through controlled variations of the crystal growth rate, i.e. a rate grown crystal.

Also a semiconductor wafer having zones of alternate conductivity type and of somewhat the same configuration as that shown in Fig. 1 may be produced by the alloy process wherein a wafer of single conductivity type is baked with each surface of the wafer in contact with a small amount of impurity material producing a conductivity type opposite that of the wafer. The baking is at a temperature above the melting point of the impurity and for a time sufficient to allow the impurity to alloy with all of the material of the wafer except for a small narrow zone through the middle of the wafer.

By still another method, extremely thin layers of two impurities producing opposite types of conductivity and having different diffusion rates are deposited on one side of a wafer of single conductivity type by a vapor deposition process. The wafer is thereafter baked at a temperature below the alloying temperature for a time sufficient to allow the impurities to diffuse a short distance into the wafer. Since the two impurities have different diffusion rates, one will penetrate the wafer to a greater extent than the other and alternating zones of opposite conductivity types are produced.

All of the above briefly described methods for producing junction transistor blocks are now well-known in the art and no further explanation is believed necessary. All of these methods, and others known in the art, are applicable to the practice of the present invention.

In practicing the present invention, the transistor wafer or block of Fig. 1 is further prepared as illustrated in Fig. 2 by making a depression 13 in the center of the bottom layer 11 with the depression extending almost to the intermediate layer 12, so that its bottom forms an imperforate zone of small but appreciable thickness. In conventional transistor terminology, the bottom layer 11 is referred to as the collector side, the top layer 10 is referred to as the emitter side and the intermediate layer 12 is referred to as the base layer or region. Thus, it will be evident that the depression 13 is formed on the collector side and extends into the wafer nearly to the base layer or region 12.

After the depression 13 has been made in the collector layer, a base contact wire is alloyed into the base layer or region through the bottom of the depression. Whereas the base contact wire is shown as being connected to the base region from the collector side of the unit it will be appreciated that it will also be possible to effect the base contact connection from the emitter side of the unit. In these circumstances, the depression 13 will not be formed in layer 11, but rather in layer 10.

In making the base connection, it is essential to obtain good electrical contact. If the base layer or region be of p-type conductivity and layers 10 and 11 be of n-type conductivity, then the alloying end of the base contact wire should likewise be consistent with the type of conductivity of the various layers by producing p-type conductivity. Thus, for example, it is possible to utilize in the case of a p-type base region, a material such as aluminium producing p-type conductivity as the material of the lead wire 14 and to bond the wire to the base region through the small amount of material which lies between the base region and the bottom of the depression 13. In the process, the tip of the wire 14 is pressed against the bottom of the depression 13 and the semiconductor block heated. When the proper temperature is reached, the semiconductor material underlying the tip of the wire 14 will soften and melt as will the aluminium at the tip of the wire 14 and all the ingredients will mix together permitting the wire 14 to move

inwardly slightly nearer to the base region. Thereafter, as the semiconductor block is cooled, the molten mixture of materials will solidify in the form of a mass of semiconductor material, aluminium and the small amount of n-type material which initially was contained in the semiconductor material since this material was part of layer 11. The resulting conductivity of the mass, designated by the numeral 15 in Fig. 3, is of p-type due to the presence of the aluminium which overbalances the small quantity of n-type material. Thus, there is produced by this technique a connection to the base region 12 by means of an intermediate alloy material which imparts to the connection the same type of conductivity as the base region 12.

At this point it should be noted that it is highly desirable although, as mentioned above, not absolutely essential to form this contact from the collector side of the transistor rather than from the emitter side and to prevent the alloy material 15 from extending into the emitter region and converting any portion of that region into p-type material.

The reason for this lies in the relationship between reverse "breakdown" voltage across a p-n junction and the resistivity of the two regions. A reasonably close approximation for this relationship for silicon, is given by the formula $E_z = 39P_n + 8P_p$, where E_z is the Zener or "breakdown" voltage. P_n is the resistivity of the n region and P_p is the resistivity of the p region. The approximate formula for the Zener voltage of germanium assumes the same form as the formula above but involves different constants. Thus, for example, the maximum reverse voltage which may be applied between the emitter and base of an n-p-n silicon transistor with an emitter resistivity of 0.01 ohm-centimeter, a base resistivity of 1.0 ohm-centimeter, and a collector resistivity of 2.0 to 3.0 ohm-centimeters, all within the usual range for junction transistors, would be approximately 8.4 volts. In the same transistor, the maximum base-collector reverse bias voltage would be approximately 80 to 120 volts. However, alloying a high concentration of p-type impurity material into the junction region produces a region of much lower resistivity, say for example, 0.1 ohm-centimeter. The above formula now reveals that if this low resistivity p region extends far enough to contact both the emitter and the collector regions, the maximum reverse voltages are reduced almost to one volt between the emitter and the base and to about 70 volts between the collector and the base.

Thus, it can be seen that the effect on the emitter-base reverse voltage is tremendously greater percentage-wise than the effect on the collector-base reverse voltage. By this example it can be seen that the performance characteristics of the transistor are greatly enhanced if the alloy forming the base contact connection is not allowed to form part of the emitter-base junction. This same thing is true of p-n-p transistors although to not nearly so great an extent.

It has been assumed in the foregoing discussion that the base region is of p-type conductivity. Under these conditions it is possible to use an alloy of a neutral impurity metal, that is, one producing no change in the type of conductivity of the semiconductor material, such as gold, lead, silver, tin, platinum etc. with one of the p-type impurities such as boron, gallium, thallium, or indium as the material of lead wire 14. Alternately, only the tip of wire 14 need be made of such an alloy or even the tip of wire 14 only coated with a material producing p-type conductivity. On the other hand, if the base region 12 is of n-type conductivity, then it will be necessary to use an alloy of a neutral impurity metal with one of the n-type impurity materials as set forth in the preceding discussion. The alloy should contain from about 95% to about 99.9% of a neutral impurity metal and from about 0.1% to about 5.0% of the impurity material.

The connections to the outer layers 10 and 11 may be effected by any conventional means which will produce the necessary electrical contact. Thus, for example, regions of the surfaces of the layers 10 and 11 may be roughened, such as by sand blasting, and subsequently these roughened regions nickel plated. Thereafter lead wires may be conveniently soldered to the nickel coatings. Alternatively, a convenient way for making connection to the two outer layers 10 and 11 would be to utilize an intermediate ingredient which combines well with the material of the lead wire to be used and the layers 10 and 11. Such an intermediate material could be gold. Other materials, however, will be apparent to those skilled in the art. To this end, it is simply necessary to place a coating, for example, gold, on each of the lead wires and thereafter to press the lead wires against the surfaces of the outer layers 10 and 11 while heating the semiconductor material thereby making good contact. If the intermediate material is a neutral impurity, then it should be doped with an impurity of the same type as contained in layers 10 and 11. For example, if layers 10 and 11 and of n-type conductivity, then the gold can conveniently be doped with antimony.

Prior to initiating the method of the present invention, it is preferred that the semiconductor block or wafer be cleaned. This can be accomplished by using a standard etch solution, as for example a solution comprising 200 cc. of nitric acid, 120

cc. each of hydrofluoric acid and acetic acid and 44 drops of bromine, commonly known as CP-4, or any equivalent. It may also be necessary in order to clean completely the semiconductor wafer to subject it to ion bombardment in a vacuum.

There is illustrated in Fig. 4 an arrangement particularly suitable for large area junction transistors. In this particular embodiment of the invention, three distinct lead wires 20, 21 and 22 are connected to the base region 12 by the techniques above described. By this means, connection is made to distinct points in the base layer whereby the effect of poor lateral conductance of the base layer 12 is minimized and the current density equalized to some extent by dividing the base current among the several contacts. Accordingly, by effectively reducing the resistance in the base layer in this manner, it no longer need be considered as a limiting factor in the operation of the transistor.

There is not to be precluded from the present invention the definition of one or a plurality of recesses 13 in each of layers 10 and 11 at the same time and in the same transistor. This arrangement would be highly advantageous in securing the maximum possible number of connections to base layer 12.

In Fig. 5 there is illustrated the manner in which connection is made to the base layer of a very thin slab such as may be produced by the diffused junction technique. As will be evident, a transistor slab is shown comprised essentially of outer layers 25 and 26 constituting the emitter and collector layers and an intermediate layer 27 constituting the base region or layer. Since the transistor is formed as a very thin slab, the layers 25 and 26 are quite thin and accordingly it is possible to make connection to base layer 27 directly through any chosen part or zone of either or both of layers 25 and 26 without first forming a depression as was done in connection with Figs. 1 to 4. In this embodiment it is also desirable, as shown above, to prevent the base connection alloy from forming part of the emitter-base junction. There is further shown in Fig. 5 a wire 28 attached to base layer 27 by a mass 29. The materials and their selection in this embodiment are consistent in all respects with the attachment of wire 14 to base layer 12. Whereas the thin slab illustrated in Fig. 5 will have superior electrical properties it will be mechanically more fragile before and during fabrication prior to mounting.

WHAT WE CLAIM IS:—

1. A method of making a junction type transistor comprising two outer layers of the same conductivity type with an intermediate base layer of opposite conductivity type therebetween, wherein an electrical connection is made to said base layer by the steps of providing in one outer layer an alloying zone which is joined to the base layer and which has a small but appreciable thickness, and alloying through said alloying zone a lead wire comprised of a material which produces the same conductivity type as said base layer to form the required electrical connection.

2. A method of making a junction type transistor according to Claim 1, wherein said alloying zone comprises a recess in one of said outer layers, with the bottom of the recess being spaced by a small but appreciable thickness from the intermediate base layer of the transistor.

3. A method as claimed in Claim 1 or 2, wherein that outer layer into which the base connection is alloyed is the collector layer.

4. A method as claimed in any preceding claim, wherein the outer layers are formed of n-type material and the intermediate layer is formed of p-type material and the lead wire is comprised of material which produces p-type conductivity.

5. A method as claimed in any of Claims 1 to 3, wherein the outer layers are comprised of p-type material and the intermediate layer is formed of n-type material and the lead wire is comprised of material which forms n-type conductivity.

6. A method as claimed in any of Claims 1 to 5, wherein the alloying is effected by utilizing an additional material which is combined with the material of the lead wire as well as the impurity material.

7. A method as claimed in Claim 6, wherein said additional material comprises a neutral impurity metal and n-type impurity.

8. A method as claimed in Claim 6, wherein the additional material comprises a neutral impurity metal and a p-type impurity.

9. A method as claimed in Claim 1, wherein said alloying zone comprises a region of said one outer layer with a thickness equal to the thickness of the said one outer layer.

10. A method as claimed in any of Claims 1 to 9, wherein a plurality of recesses are defined in one of the collector and emitter layers and a lead wire is alloyed through the bottom of each of said recesses to the base layer.

11. The improved method of making a base connection to a junction transistor substantially as described with reference to the accompanying drawings.

12. A junction transistor made by the method according to any of the preceding claims.

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2. A method of making a junction type transistor according to Claim 1, wherein said alloying zone comprises a recess in one of said outer layers, with the bottom of the recess being spaced by a small but appreciable thickness from the intermediate base layer of the transistor.

3. A method as claimed in Claim 1 or 2, wherein that outer layer into which the base connection is alloyed is the collector layer.

4. A method as claimed in any preceding claim, wherein the outer layers are formed of n-type material and the intermediate layer is formed of p-type material and the lead wire is comprised of material which produces p-type conductivity.

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11. The improved method of making a base connection to a junction transistor substantially as described with reference to the accompanying drawings.

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