

FIG.1

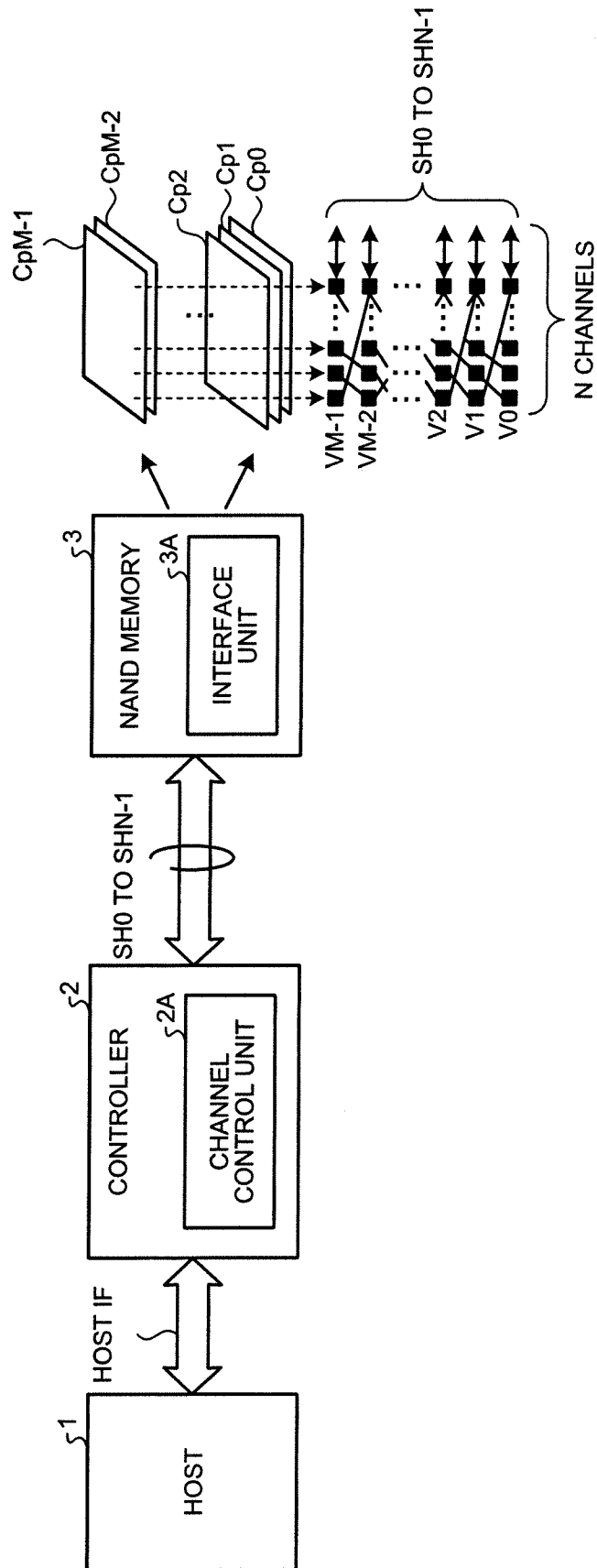


FIG.2

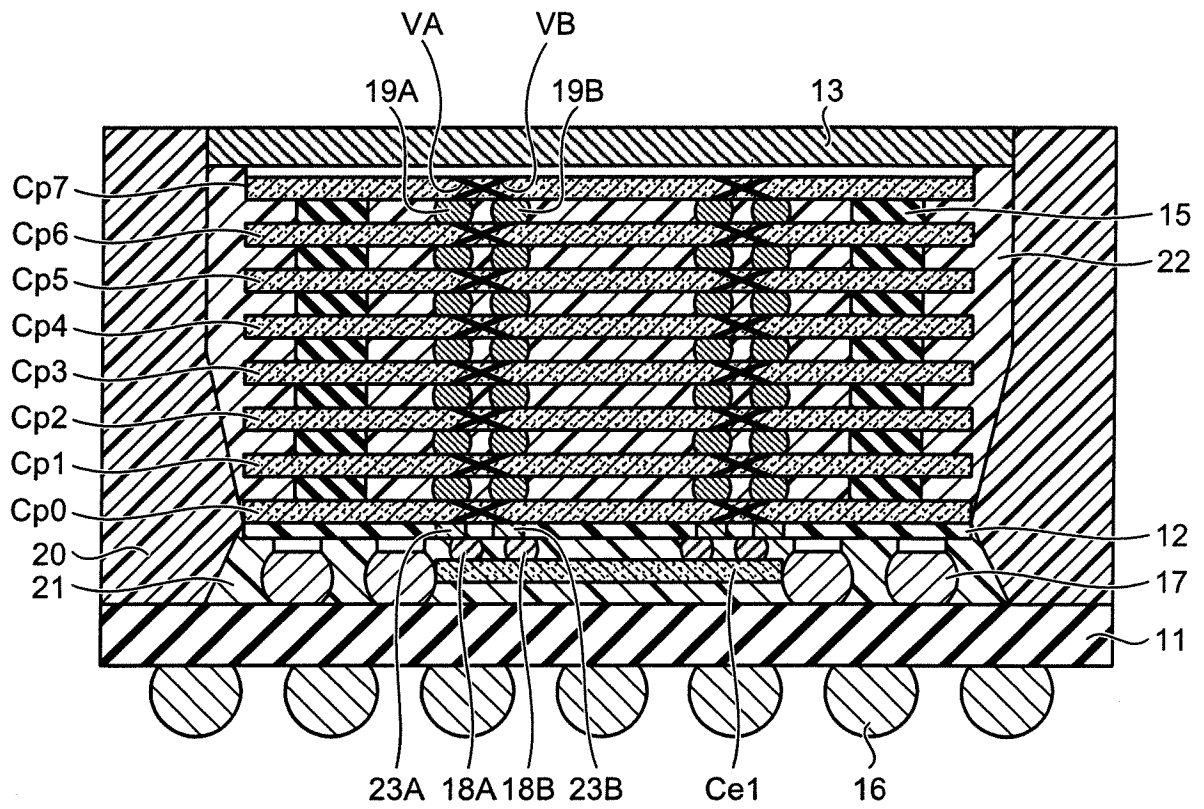


FIG.3

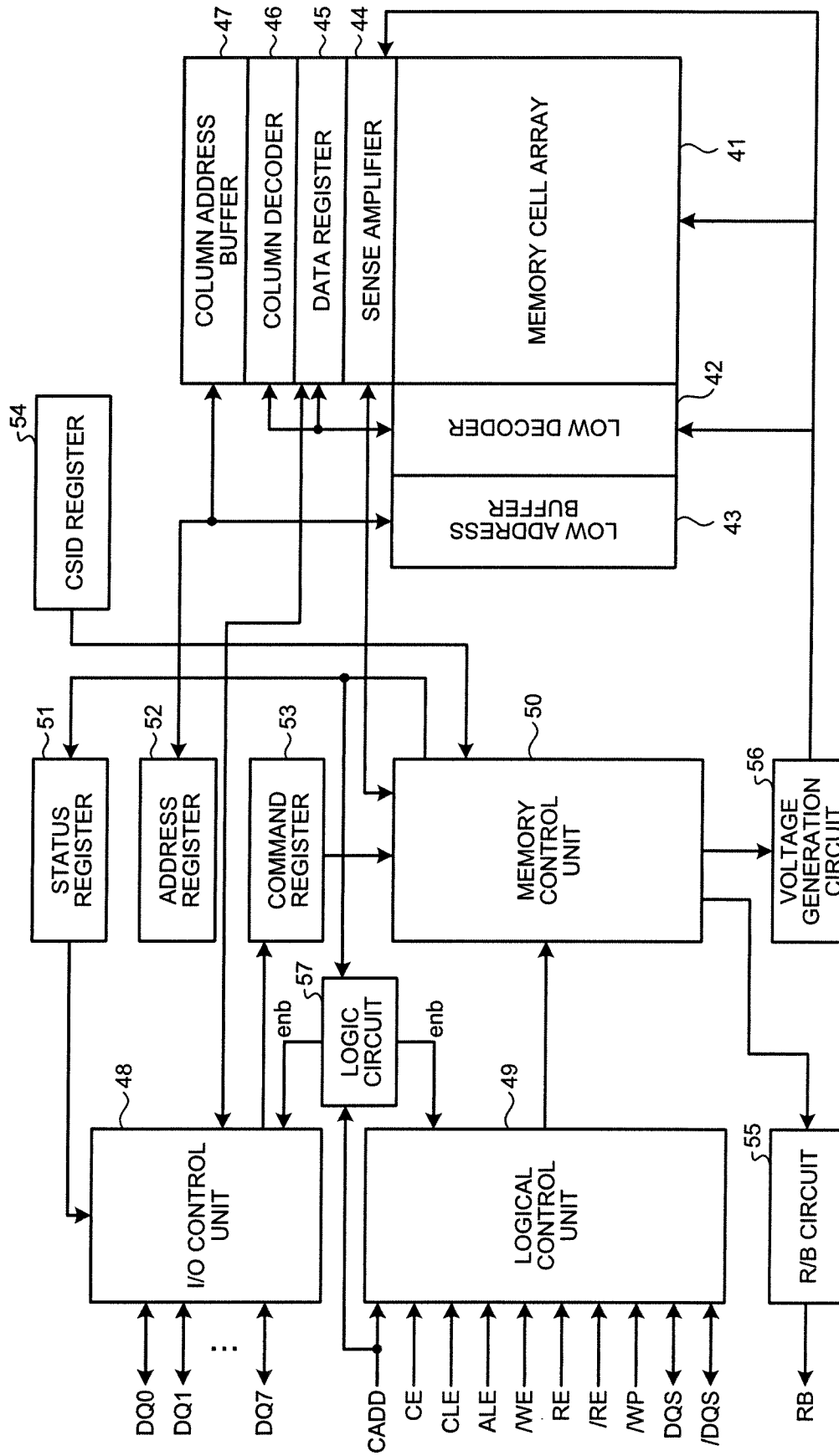


FIG.4

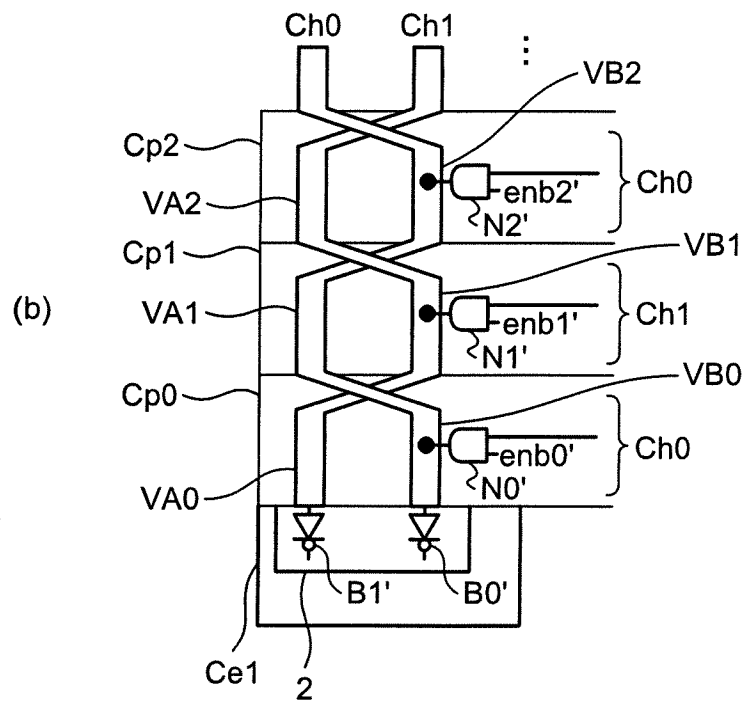
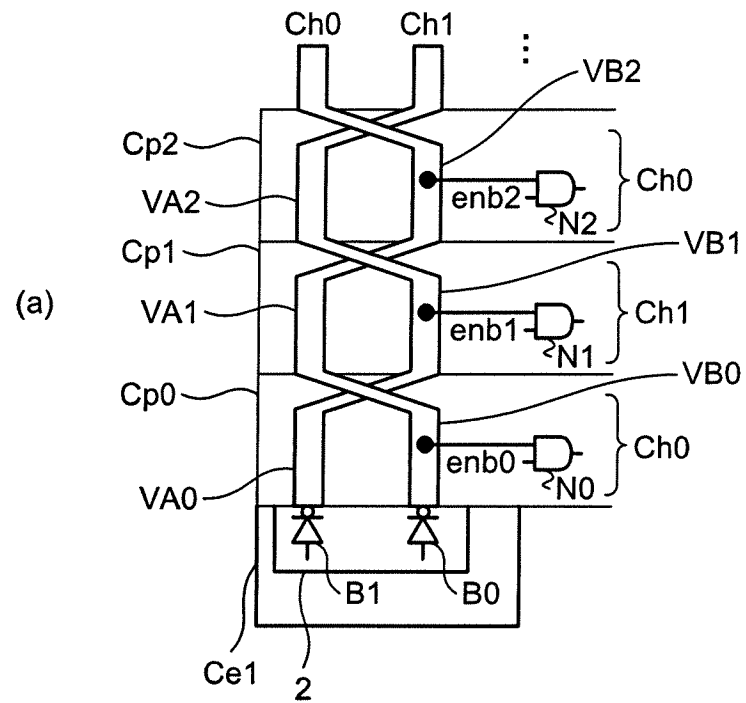


FIG.5

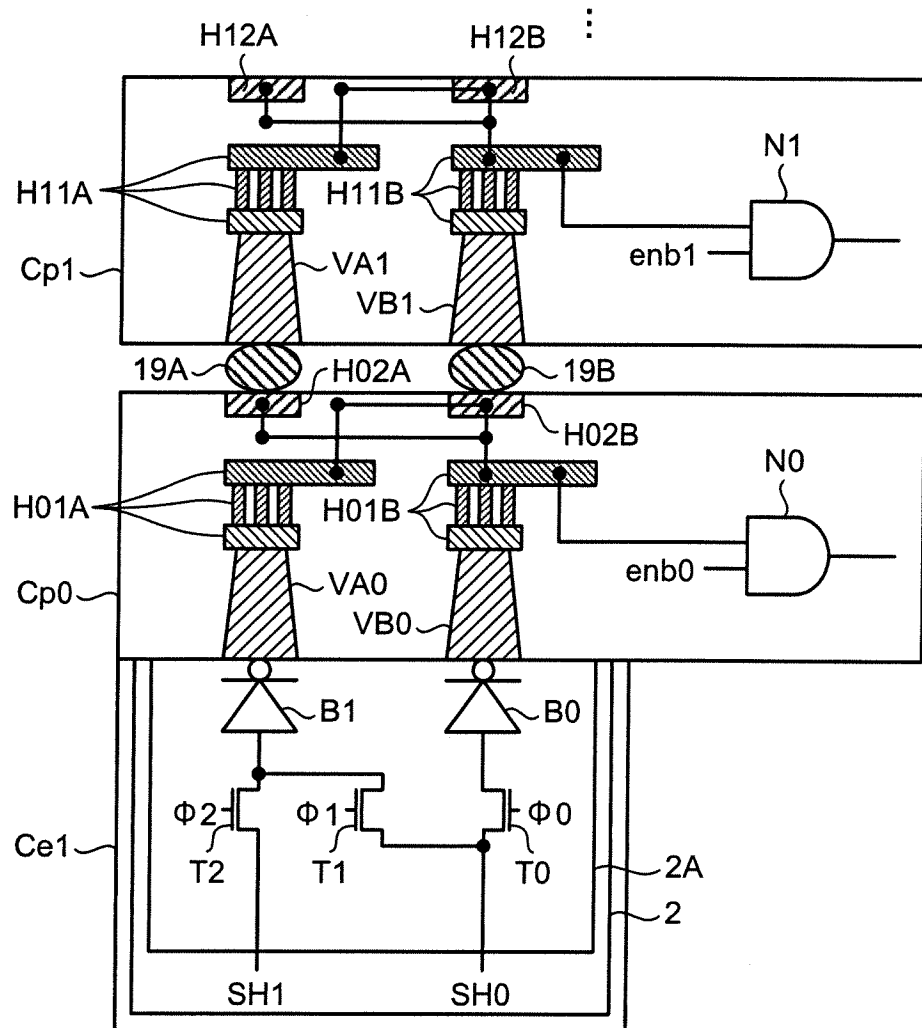


FIG.6

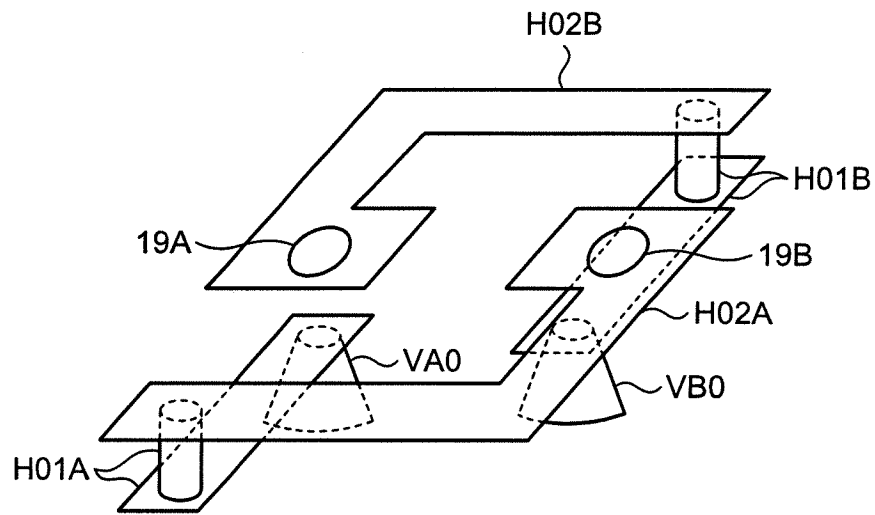


FIG.7

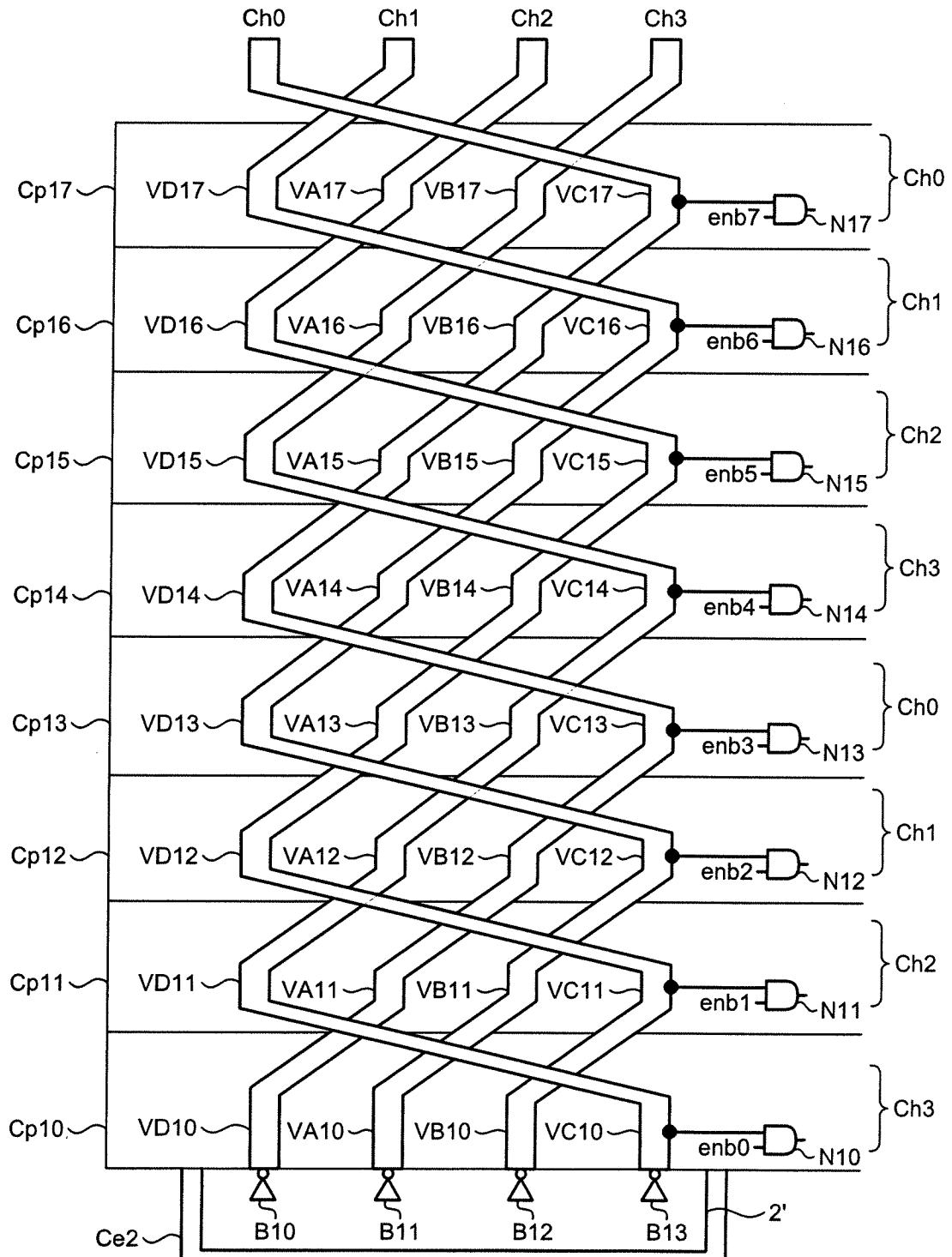


FIG.8

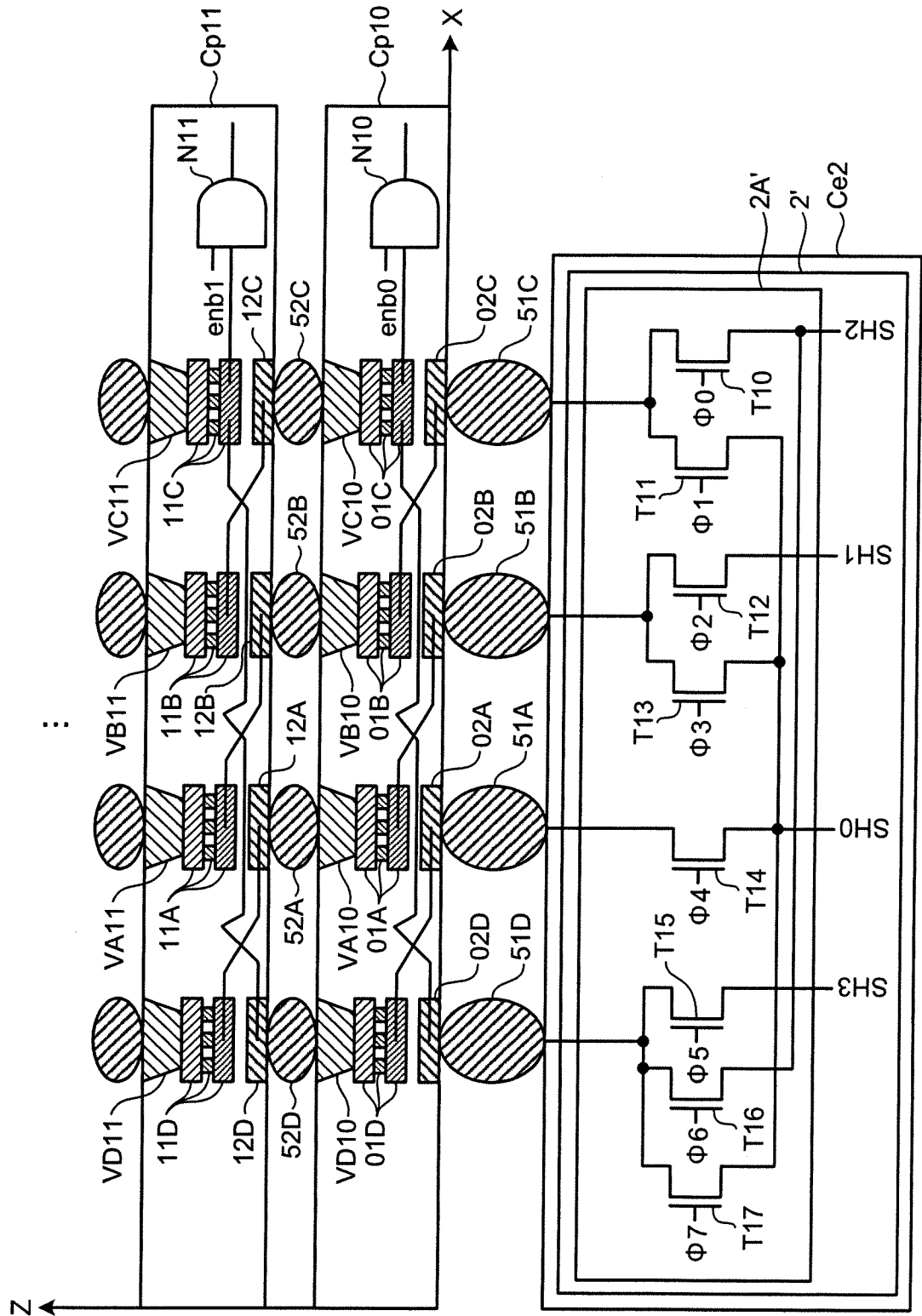


FIG.9

CH: CHANNEL CE: CHIP ENABLE	SH0	SH1	SH2	SH3
1CH/1CE	CE0			
1CH/2CE	CE0		CE2	
1CH/4CE	CE0	CE1	CE2	CE3
EACH 2CH/1CE	CE0		CE2	
EACH 2CH/2CE	CE0	CE1	CE2	CE3
EACH 4CH/1CE	CE0	CE1	CE2	CE3

Figure 1 consists of five plan views (a) through (e) of a semiconductor device, showing the progression of a manufacturing process. Each view includes an X-axis and a Y-axis.

- (a) Shows a substrate with four rectangular regions: 11A (top-left), 11B (top-right), 11C (bottom-left), and 11D (bottom-right). Regions 11A and 11B are shaded with diagonal lines, while 11C and 11D are unshaded.
- (b) Shows regions 11A and 11B with additional features 11A' and 11B' (indicated by dashed lines). Regions 11C and 11D are also shown with additional features 11C' and 11D' (indicated by dashed lines).
- (c) Shows regions 11A and 11B with additional features 11A' and 11B' (indicated by dashed lines). Regions 12A and 12B are shown with additional features 12A' and 12B' (indicated by dashed lines).
- (d) Shows regions 11A and 11B with additional features 11A' and 11B' (indicated by dashed lines). Regions 12A and 12B are shown with additional features 12A' and 12B' (indicated by dashed lines).
- (e) Shows regions 11A and 11B with additional features 11A' and 11B' (indicated by dashed lines). Regions 12A and 12B are shown with additional features 12A' and 12B' (indicated by dashed lines).

