

"A SEMICONDUCTOR MEMORY DEVICE"

The present invention relates to a semiconductor memory device, and more particularly to a semiconductor memory device having a one-transistor type memory cell in which one transistor and one capacitor are connected in series.

A dynamic type RAM (Random Access Memory) is now extensive by used practice in the RAM employing a one-transistor type memory cell in which one insulated gate type field effect transistor (hereinafter referred to as a "MISFET") and one capacitor are connected in series. A theme on the manufacturing technology of this dynamic RAM is to reduce to the utmost the occupying area of the capacitors of a large number of memory cells which are formed on a semiconductor substrate. As a solution for reducing the occupying area of the capacitors, it is considered to use a material of higher permittivity as a dielectric material which constitutes the capacitors. Previously a silicon oxide film has been common as the dielectric material put into practical use. It is considered to replace this material with a silicon nitride film of high permittivity. The silicon nitride

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film has a permittivity which is about double that of the silicon oxide film, and owing to which a substantial decrease in the occupying area relative to that of the conventional capacitor employing the silicon oxide film can be expected.

As the result of experimental researches, we have discovered the problem that, when a capacitor is formed on the surface of a semiconductor substrate by employing the silicon nitride film as the dielectric material between the two electrodes of the capacitor, the surface state of the semiconductor substrate surface changes to vary the value of capacitance of the capacitor, in accordance with the magnitude and polarity of a voltage applied across the electrodes. More specifically, our experimental researches have revealed that, in the case where a silicon oxide film is formed on the surface of a semiconductor substrate and is further overlaid with a silicon nitride film so as to use both the films as the dielectric film of a capacitor, unfavourable carriers are accumulated in a trap region formed in the dielectric film, in accordance with the magnitude and polarity of the applied voltage, and they change the state of the semiconductor substrate surface, thereby producing

a variation-with-time in the value of capacitance of the capacitor. The variation in the value of capacitance of the capacitor is liable to cause a soft error or malfunction of a memory device, and results in limiting the lifetime during
5 which the memory device performs normal operations.

The present invention has been made on the basis of the finding of the above referred to problem of voltage-dependency involved when a dielectric film of high permittivity is used.

10 It is an object of the present invention to prevent the deterioration of characteristics attributed to the voltage-dependency in a memory device having a memory cell in which a data storage capacitor is formed of a dielectric film having a high permittivity such as silicon
15 nitride film.

According to a first aspect of the present invention there is provided a semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:-

20 (a) a memory cell which includes a series connection consisting of a switching MISFET and a storage capacitor, said storage capacitor consisting of a semiconductor region of a semiconductor substrate, a silicon nitride film formed over a surface of said semiconductor
25 region, and a conductive layer formed over said silicon nitride film;

(b) a bit line which is connected to one end of said series connection and which supplies a signal voltage and;

30 (c) a terminal which is connected to the other end of said series connection and which supplies a voltage to said other end of said series connection so that a voltage of said storage capacitor to be stored between said semiconductor region and said conductive layer may become
35 smaller in an absolute value than the signal voltage supplied to said bit line.

According to a second aspect of the present invention there is provided a semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:

5 a memory cell which includes a series connection comprised of a switching MISFET and a storage capacitor connected in series, said storage capacitor being comprised of a first conductive layer formed over a semiconductor region of a semiconductor substrate, a silicon nitride film
10 formed over said first conductive layer and a second conductive layer formed over said silicon nitride film;

a bit line which is connected to one end of said series connection and which supplies a signal voltage having a predetermined high level V_H and a predetermined low level
15 V_L to said memory cell; and

a terminal which is connected to the other end of said series connection and which supplies a voltage V_p which is greater than V_L but less than V_H to said other end of said series connection so that a voltage V_s of said storage
20 capacitor to be stored between said first conductive layer and said second conductive layer has a smaller absolute value than the absolute value of V_H supplied to said bit line.

According to a third aspect of the present
25 invention there is provided a semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:

a memory cell which includes a series connection comprised of a switching MISFET and a storage capacitor
30 connected in series, said storage capacitor being comprised of a first conductive layer formed over a semiconductor region of a semiconductor substrate, a silicon nitride film formed over said first conductive layer and a second conductive layer formed over said silicon nitride film;

35 a bit line which is connected to one end of said series connection and which supplies a signal voltage

having a predetermined maximum value to said memory cell;
and

5 a terminal which is connected to the other end of
said series connection and which supplies a voltage to said
other end of said series connection so that the voltage to
be stored by said storage capacitor is either positive or
negative and substantially less in absolute magnitude than
the maximum swing in the signal voltage supplied to said
bit line.

10 According to a fourth aspect of the present
invention there is provided a semiconductor memory device
formed at a major surface of a semiconductor substrate,
said memory device including:

(a) a storage capacitor formed therein, said
15 capacitor having a pair of electrodes and at least a silicon
nitride film located therebetween;

(b) a terminal connected to a first electrode for
applying a specified voltage thereto;

(c) means for applying either one of two logic
20 level voltages to said second electrode;

whereby said specified voltage has a relationship
with the two logic level voltages that said capacitor can
store either a positive voltage or a negative voltage
depending on which logic level voltage is applied to
25 second electrode.

According to a fifth aspect of the present
invention there is provided a semiconductor memory device
formed at a major surface of a semiconductor substrate,
said memory device including:

30 (a) a storage capacitor formed therein, said
capacitor having first and second electrodes and at least
a silicon nitride film formed between said electrodes;

(b) a terminal for applying a first voltage to
the first electrode;

35 (c) means for applying one of second and third
voltages to the second electrode;

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wherein the absolute value of the resultant voltage applied across the two electrodes of the storage capacitor is smaller than the absolute value of the difference between the second and third voltages.

5 The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a sectional view showing the structure of a preferred form of a memory cell in a
10 semiconductor memory device;

Figure 2 is an equivalent circuit diagram of the memory cell shown in Figure 1;

Figure 3 is a graph showing the relationship between the stress voltage V_S and the change ΔV_{FB} of the
15 flat band voltage;

Figure 4 is a graph showing the relationship between the stress voltage V_S and the time T for changing ΔV_{FB} to a predetermined value;

Figure 5 is a circuit diagram showing a
20 preferred form of semiconductor memory device;

and

Figure 6 is a graph to assist in explaining the operation of the circuit shown in Figure 5.

Figures 1 and 2 show an embodiment of a dynamic RAM according to the present invention wherein a series circuit consisting of a switching MISFET and a storage capacitor is formed as a memory cell on a semiconductor substrate. First, the memory cell portion will be described with reference to Figure 1.

With reference to Figure 1, letter C designates a part where the storage capacitor of the memory cell is formed, and letter Q designates a part where the switching N-channel MISFET connected in series with the capacitor C is formed. The switching MISFET Q includes a thin gate insulator film 10 which is formed on the major surface of a P-type semiconductor substrate 1, and a gate electrode 11 which is formed thereon. A P-type single crystal silicon substrate having, e.g. the (100) plane surface, is used as the substrate 1, and a silicon oxide (SiO_2) film is used as the gate insulator film 10. In addition, a polycrystalline silicon film is used as the gate electrode 11. In the substrate 1, N^+ -type semiconductor regions 8 and 9 are formed so as to define the channel region of the MISFET Q.

Both these regions operate as source and drain regions, or drain and source regions.

The capacitor portion C has an N^+ -type semiconductor region 7 which is formed adjacent the semiconductor region 8 operating as the drain or source region. This region 7 has a predetermined occupying area in accordance with a capacitance value required of the capacitor, and forms one electrode of the capacitor.

10 A thin silicon oxide film 2 is formed on the region 7. This silicon oxide film is intended to relieve a stress on the substrate surface ascribable to the difference of the coefficients of thermal expansion of a silicon nitride (Si_3N_4) film to be formed thereon and the substrate 1, in order to prevent crystal defects from developing.

A silicon nitride film 3 is formed on the silicon oxide film 2. Furthermore, a thin silicon oxide film 4 is formed on the silicon nitride film 3, and a counter electrode 5 of the capacitor is formed of polycrystalline silicon thereon. The counter electrode 5 is opposite the region 7, and has an occupying area substantially equal to that of the latter. This electrode 5 may well be formed integrally with a wiring lead which extends on the semiconductor substrate. A thick silicon oxide film (field silicon

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oxide film) 6 is formed between the cell forming regions.

In this structure, the silicon nitride film 3 having a high permittivity is employed as the dielectric film of the capacitor, so that the occupying area of the capacitor forming portion C can be reduced. In one form the silicon nitride film may be formed directly on the region 7 of the substrate 1. As described above, however, when the silicon nitride film is formed directly on the surface of the region 7, the difference of the coefficients of thermal expansion of the silicon substrate and the silicon nitride film incurs a thermal strain in the surface of the silicon substrate 1 and brings about the crystal defects therein. It is therefore preferable to form the silicon nitride (Si_3N_4) film 3 through the SiO_2 film 2. Moreover, in the case where the SiO_2 film is not interposed, the interface characteristics become unstable, and quantitatively, the flat band voltage V_{FB} is changed to cause variation-with-time in the capacitance (C) - voltage (V) characteristic. Furthermore, a leakage current takes place, and the breakdown voltage is reduced. It is therefore favourable to form the Si_3N_4 film 3 through the SiO_2 film 2.

In the above described memory cell device,
a terminal P_1 is connected to the electrode 5
of the capacitor C. A specified voltage V_p
is applied through this terminal P_1 . As
5 illustrated in Figure 2, the voltage V_p
is determined according to a voltage which is
applied to a bit line (data line) BL with the memory
cell connected thereto, in correspondence with the
logic level "1" or "0" of data. Letting V_H
10 denote the voltage of the logic "1" to be applied
to the bit line BL, and V_L denote the voltage
of the logic "0", the voltage V_p is determined
by the relationship of $V_L < V_p < V_H$. In
particular, to the end of applying equal voltages
15 for both the positive and negative signs of a
voltage which is applied to the semiconductor
substrate electrode 7 of the capacitor C, the
voltage V_p should desirably be set at
$$V_p = \frac{V_H + V_L}{2}$$

By way of example, when the
20 voltage of the bit line BL changes between $V_H = +5$ V
and $V_L = 0$ V, it is desirable to set
 $V_p = +2.5$ V. In the case of setting $V_p = +2.5$ V,
a voltage V_s which is applied across both the
electrodes (5, 7) of the capacitor at $V_H = +5$ V
25 becomes +2.5 V, so that the substrate electrode

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7 is positively biased with respect to the substrate
5. Conversely, the voltage V_S applied across both
the electrodes of the capacitor at $V_H = 0$ V becomes
-2.5 V, so that the substrate electrode 7 is
5 negatively biased with respect to the electrode 5.

As a result of the above, the voltage V_S
to be applied across both the electrodes (5, 7) of
the capacitor C (hereinafter, this voltage will
be referred to as the "stress voltage") is rendered
10 as small as possible for the voltages of both
the positive and negative signs. The reason
therefor will be clarified from the ensuing
description.

First, we have discovered that the
15 following phenomenon arises in the capacitor C which
uses the silicon nitride film as the dielectric
film.

Figure 3 is a graph showing the result of
an experiment which was conducted on the relation-
20 ship between the stress voltage V_S (V) and the flat
band voltage V_{FB} (V) serving as an indicator for
a surface charge state, as to the capacitor
structure wherein similarly to the capacitor C
shown by the embodiment of Figure 1, an Si
25 substrate was successively formed thereon with SiO_2
film Si_3N_4 film, SiO_2 film and a polycrystalline

silicon layer. The positive stress voltage V_S denotes that the semiconductor substrate electrode 7 becomes a positive voltage with respect to the electrode 5, whereas the negative stress voltage V_S denotes that the substrate electrode 7 becomes a negative voltage with respect to the electrode 5.

In the above experiment, the thickness of the silicon nitride film 3 was $180 \text{ \AA}$, and that of the uppermost silicon oxide film 4 was $20 \text{ \AA}$.

Further, the thickness of the lowermost silicon oxide film 2 was varied between the values of $110 \text{ \AA}$, $150 \text{ \AA}$ and $210 \text{ \AA}$. The stress voltage V_S was applied at room temperature for 1 minute. Curves A, B and C in Figure 3 correspond to samples in which the lowermost silicon oxide films (SiO_2) were $110 \text{ \AA}$, $150 \text{ \AA}$ and $210 \text{ \AA}$ thick, respectively.

As illustrated in Figure 3, even when the stress voltage V_S changes, the flat band voltage V_{FB} does not change and is substantially flat in a range R_1 . In contrast, the flat band voltage V_{FB} varies for higher stress voltages V_S , and it deviates from the flat state outside the range R_1 .

Upon further studying the above phenomenon, we have observed at a measurement temperature of 125°C the relationship between the positive stress voltage V_S (V) and the period of time T (minutes)

in which ΔV_{FB} changes predetermined values (here, 30 mV and 100 mV). Figure 4 illustrates the variations of V_{FB} depending upon the stress voltage V_S . A straight line A in Figure 4 has been obtained by plotting the periods of time in which ΔV_{FB} became - 30 mV, and a straight line B by plotting the periods of time in which ΔV_{FB} became -100 mV, in relation to the stress voltage V_S .

It will be noted from Figure 4 that, with an increase in the stress voltage V_S , the period of time in which ΔV_{FB} changes to the predetermined value shortens. It has accordingly been known from Figure 4 that, in the capacitor employing the silicon nitride film as the insulating film, the operation with a lower stress voltage or lower applied voltage changes the surface state less.

The reason for this is as stated below. In the case of using the silicon nitride film, a region (trap level) which traps charges is formed in the Si_3N_4 film, and the charges are stored at the trap level by the applied voltage, so that the surface state of the semiconductor substrate constituting the capacitor changes. The change of V_{FB} results in the change of the value of capacitance of the capacitor. This change varies greatly in accordance with the time of application of the stress voltage V_S . In

consequence, a great capacitance change is exhibited with respect to a predetermined initial value, and the function as the capacitor of the memory cell is spoilt. The cause of this is considered to be that the stored charges of the trap level will change with a lapse of time. The variation of the capacitance value, namely, that of ΔV_{FB} becomes greater as the stress voltage is larger.

As revealed from the above results illustrated in Figures 3 and 4, the function as a memory cell can be increased as a result of the reduction in the stress voltage applied across both the electrodes of the capacitor.

In principle, the voltages for the capacitor C in both polarities are rendered the smallest possible applied voltages. That is, when the voltage V_p (memory cell electrode voltage) to be applied to one electrode of the capacitor C via the terminal P_1 is determined by the relationship of $V_L < V_p < V_H$ as described above, the voltage V_g to be applied across the capacitor can be reduced to a low level for the voltages of both polarities.

Especially in the case where the voltage V_p is determined by the equation $V_p = \frac{V_L + V_H}{2}$ equal voltages can be applied for the voltages of both polarities.



Consider by way of example that, in the case of operating the memory device, the high level ("1" level) V_H of the bit line BL is 5 V, while the low level ("0" level) V_L is 0 V. Then, in the case where the memory cell electrode voltage V_P has been set at $\frac{V_L + V_H}{2} = 2.5$ V, the stress voltages V_S of the capacitor C can be reduced to 2.5 V in the absolute value as indicated in the following table:

	<u>LOGIC LEVEL</u>	<u>$V_P = + 2.5$ V</u>
10	$V_H = + 5$ V	$V_S = + 2.5$ V
	$V_L = 0$ V	$V_S = - 2.5$ V.

Whilst, in the above, the memory cell electrode voltage V_P has been exemplified as being halved, this applied voltage V_P may be selected on the basis of a supply voltage (which substantially determines the V_H level). For example, in the case of setting V_P at + 1 V, V_S can be limited within a range of - 1 to + 4 V, and in the case of setting V_P at + 4 V, V_S can be limited within a range of - 4 V to + 1 V. The stress voltage may be selected within the range R_1 shown in Figure 3 within which ΔV_{FB} does not rise, and the voltage V_P may be set at a voltage level intermediate between the high and low logic levels.

25 The present invention is also applicable to a silicon nitride dielectric film which has the



so-called voltage-dependency in order to render the surface state of a semiconductor substrate surface unstable, depending upon the magnitude of a voltage of the direction of an electric field. The electric field of the capacitor portion of a memory cell is optimized, whereby enhancement in the reliability and enhancement in the breakdown voltage can be achieved. Furthermore, the capacitance electrodes of a one-transistor type RAM can be rendered smaller, which is effective for enlarging the capacitor of the one-transistor RAM.

Figure 5 shows a circuit diagram of the above described semiconductor memory device constructed on a single semiconductor substrate by employing the memory cells as described above. The memory device includes the memory cell portion M-CELL referred to above, the memory cells being arrayed in the shape of a matrix. A sense circuit SA is composed of N-channel MISFETs $Q_1 - Q_5$, which sense circuit is controlled by a control pulse signal ϕ_2 . Each sense circuit is coupled to one pair of adjoining bit lines BL_1 and $\overline{BL_1}$ (BL_2 and $\overline{BL_2}$). A dummy cell D-CELL is coupled to each bit line, and is composed of a MISFET Q' and a capacitor C' in similar manner to the memory cell. However, the value of capacitance of the

capacitor C' of the dummy cell D-CELL is set at about $\frac{1}{2}$ of that of the capacitor C of the memory cell M-CELL. The capacitor C' can be formed by the same structure as that of the capacitor C of the memory cell described above.

The memory device also includes word lines $WL_1 - WL_6$ which are coupled to the memory cells or dummy cells arrayed in the respective rows, an active restore circuit AC, and a precharge circuit PC constructed of an N-channel MISFET Q_6 which is driven by a control signal ϕ_1 .

In this circuit arrangement, a supply voltage V_{DD} is set at +5 V by way of example. Since the supply voltage V_{DD} substantially specifies the high level V_H of the logic levels of the bit line BL to +5 V, the voltage V_p to be applied to the terminal P_1 is set at +2.5 V, in order to reduce the stress voltage V_s of the capacitor C or C' as referred to above.

The terminal P_1 serves to supply the external voltage V_p for reducing the application of the stress voltage V_s on the capacitor. The terminals P_1 of the capacitors C and C' arranged in the matrix are connected in common and to a power supply V_p (not shown). Wiring for interconnecting the terminals P_1 can be formed by a polycrystalline silicon layer at an identical level so as to continuously extend from the

polycrystalline silicon layer 5 (Figure 1) which forms one electrode of each of the capacitors C and C'.

Referring now to the waveform diagram shown in Figure 6, t_1 indicates the point of time at which the precharge circuit PC operates, and t_2 the point of time at which a pair of predetermined word lines WL are selected to operate a specified memory cell M-CELL and a dummy cell D-CELL corresponding thereto. Further t_3 indicates the point of time at which the amplifying operation of the sense circuit SA is started, and t_4 the point of time at which the active restore circuit AC operates. As will be apparent from the operation, the pair of bit lines BL and $\overline{BL}$ have their voltage levels changed complementarily, so that terminal voltages V_{S_1} of signs opposite to each other are applied to the respective capacitors C and C' of the memory cell and the dummy cell.

Since, at this time, the voltage (2.5 V) equal to $\frac{1}{2}$ of 5 V being the high level of the bit lines is applied to one end of each of the capacitors C and C' through the terminal P_1 as described above, the voltage applied across the electrodes of each capacitor is rendered 2.5 V in the absolute value. Accordingly, the variation-with-time of the capacitors can be prevented.



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CLAIMS.

1. A semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:
 - (a) a memory cell which includes a series connection having a switching MISFET and a storage capacitor, said storage capacitor having a first conductive layer formed over a semiconductor region of a semiconductor substrate, a silicon nitride film formed over said first conductive layer, and a second conductive layer formed over said silicon nitride film;
 - (b) a bit line which is connected to one end of said series connection and which supplies a signal voltage; and
 - (c) a terminal which is connected to the other end of said series connection and which supplies a voltage to said other end of said series connection so that a voltage of said storage capacitor to be stored between said first conductive layer and said second conductive layer may become smaller in an absolute value than the signal voltage supplied to said bit line.
2. A semiconductor memory device according to claim 1, wherein said silicon nitride film is formed on a silicon oxide film which is formed on said semiconductor region.
3. A semiconductor memory device according to claim 1 or 2, wherein a voltage equal to half of said signal voltage or a voltage close thereto is applied to said terminal.



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4. A semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:

a memory cell which includes a series connection
5 comprised of a switching MISFET and a storage capacitor connected in series, said storage capacitor being comprised of a first conductive layer formed over a semiconductor region of a semiconductor substrate, a silicon nitride film formed over said first conductive layer and a second
10 conductive layer formed over said silicon nitride film;

a bit line which is connected to one end of said series connection and which supplies a signal voltage having a predetermined high level V_H and a predetermined low level V_L to said memory cell; and

15 a terminal which is connected to the other end of said series connection and which supplies a voltage V_P which is greater than V_L but less than V_H to said other end of said series connection so that a voltage V_S of said storage capacitor to be stored between said first
20 conductive layer and said second conductive layer has a smaller absolute value than the absolute value of V_H supplied to said bit line.

5. A semiconductor memory device according to claim 4, wherein

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$$V_P = \frac{V_H + V_L}{2} .$$



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6. A semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:

a memory cell which includes a series connection
5 comprised of a switching MISFET and a storage capacitor connected in series, said storage capacitor being comprised of a first conductive layer formed over a semiconductor region of a semiconductor substrate, a silicon nitride film formed over said first conductive layer and a second
10 conductive layer formed over said silicon nitride film;

a bit line which is connected to one end of said series connection and which supplies a signal voltage having a predetermined maximum value to said memory cell; and

15 a terminal which is connected to the other end of said series connection and which supplies a voltage to said other end of said series connection so that the voltage to be stored by said storage capacitor is either positive or negative and substantially less in absolute
20 magnitude than the maximum swing in the signal voltage supplied to said bit line.

7. A semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:

25 (a) a storage capacitor formed therein, said capacitor having a pair of electrodes and at least a silicon nitride film located therebetween;



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(b) a terminal connected to a first electrode for applying a specified voltage thereto;

(c) means for applying either one of two logic level voltages to said second electrode;

5 whereby said specified voltage has a relationship with the two logic level voltages that said capacitor can store either a positive voltage or a negative voltage depending on which logic level voltage is applied to second electrode.

10 8. A semiconductor memory device according to claim 7, wherein said specified voltage (V_p) is determined by the relationship $V_L < V_p < V_H$, in which V_L and V_H are respectively the logic levels 0 and 1 of data applied to said second electrode.

15 9. A semiconductor memory device according to claim 8, wherein the specified voltage is set at $(V_H + V_L)/2$.

10. A semiconductor memory device according to claim 9, wherein when said logic level voltages V_H and
20 V_L are respectively +5 and 0 volts, the specified voltage V_p is + 2.5 volts.

11. A semiconductor memory device according to claim 9, wherein when said logic level voltages V_H and V_L are respectively 0 and -5 volts, the specified
25 voltage V_p is -2.5 volts.



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12. A semiconductor memory device formed at a major surface of a semiconductor substrate, said memory device including:

(a) a storage capacitor formed therein, said
5 capacitor having first and second electrodes and at least a silicon nitride film formed between said electrodes;

(b) a terminal for applying a first voltage to the first electrode;

(c) means for applying one of second and third
10 voltages to the second electrode;

wherein the absolute value of the resultant voltage applied across the two electrodes of the storage capacitor is smaller than the absolute value of the difference between the second and third voltages.

15 13. A semiconductor memory device according to claim 12, wherein the first voltage (V_1) is determined by the relationship $V_2 < V_1 < V_3$, in which V_2 and V_3 are respectively the logic levels 0 and 1 of data applied to the second electrode.

20 14. A semiconductor memory device according to claim 13, wherein the first voltage is equal to the sum of the second and third voltages divided by two.

15. A semiconductor memory device according to claim 14, wherein said second voltage is at earth potential
25 representing a logic 0 and the third voltage is at the positive operating voltage of the memory device representing a logic 1.



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16. A semiconductor memory device according to claim 14, wherein said second voltage is at a given negative potential representing a logic 0 and the third voltage is at earth potential representing a logic 1.
- 5 17. A semiconductor memory device according to any one of the preceding claims 7 to 16, wherein the storage capacitor comprises between its two respective electrodes, a first silicon oxide film, the said silicon nitride film, and a second silicon oxide film.
- 10 18. A semiconductor memory device according to any one of the preceding claims, wherein the means for applying one of two voltages to the second electrode of the capacitor comprises a MISFET.
- 15 19. A semiconductor memory device constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.
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