

CLAIMS

What is claimed is:

1. A method of making a semiconductor device, comprising:
providing an embedded die panel comprising a plurality of semiconductor die separated by saw streets;
forming a conductive layer by an electroless plating process that comprises bussing lines disposed in the saw streets and a redistribution layer (RDL) coupled to the semiconductor die and the bussing lines;
forming an insulating layer over the conductive layer and the embedded die panel that comprises openings disposed over the conductive layer outside a footprint of the semiconductor die;
forming interconnect structures in the openings in the insulating layer by using the conductive layer as part of an electroplating process; and
singulating the embedded die panel through the saw streets after forming the interconnect structures, wherein singulating removes at least a portion of the bussing lines and forms individual fan-out wafer level packages (FOWLPs).
2. The method of claim 1, further comprising forming the embedded die panel by:
providing a carrier;
mounting the plurality of semiconductor die over the carrier; and
disposing an encapsulant around each of the plurality of semiconductor die and around a copper post coupled to each of the plurality of semiconductor die.
3. The method of claim 1, further comprising:
forming the conductive layer with a first thickness; and
forming the interconnect structures with a second thickness greater than the first thickness.
4. The method of claim 1, further comprising forming the FOWLPs comprising a thickness less than or equal to 0.6 millimeters.

5. The method of claim 1, further comprising forming the interconnect structures using a plating jig or a cover plate comprising a seal that contacts an edge of the embedded die panel and conducts current through the bussing structure to form the interconnect structures.
6. The method of claim 1, further comprising forming the conductive layer using adaptive patterning to align the conductive layer with a true position of the plurality of semiconductor die.
7. A method of making a semiconductor device, comprising:
 - providing an embedded die panel comprising a plurality of semiconductor die separated by saw streets;
 - forming a conductive layer over the embedded die panel that extends from the semiconductor die into the saw streets;
 - forming an insulating layer over the conductive layer and over the embedded die panel to comprise openings disposed over the conductive layer outside a footprint of the semiconductor die;
 - forming interconnect structures in the openings in the insulating layer by using the conductive layer as part of a plating process; and
 - singulating the embedded die panel through the saw streets to remove a portion of the conductive layer in the saw streets.
8. The method of claim 7, further comprising forming the conductive layer to include a ground pad exposed at an outer surface of the semiconductor device and at least partially overlapping the semiconductor die.
9. The method of claim 7, further comprising:
 - forming a conductive seed layer over the embedded die panel;
 - forming the conductive layer as a conductive pattern layer over the seed layer on the embedded die panel that extends from the semiconductor die into the saw streets; and
 - removing the exposed conductive seed layer from the embedded die panel.

10. The method of claim 7, further comprising forming copper posts disposed between the semiconductor die and the conductive layer.
11. The method of claim 7, further comprising forming the interconnect structures using a plating jig or a cover plate comprising a seal.
12. The method of claim 7, further comprising forming the conductive layer using adaptive patterning to align the conductive layer with a true position of the plurality of semiconductor die.
13. The method of claim 9, further comprising forming the insulating layer to comprise openings disposed over the conductive layer inside a footprint of the semiconductor die.
14. A method of making a semiconductor device, comprising:
 - providing a semiconductor die surrounded by saw streets;
 - forming a conductive layer that extends from over the semiconductor die into the saw streets;
 - forming an interconnect structure on the conductive layer; and
 - removing a portion of the conductive layer from the saw streets.
15. The method of claim 14, further comprising:
 - forming the conductive layer over a conductive seed layer by a first electroless plating process;
 - removing a portion of the conductive seed layer; and
 - forming the interconnect structure on the conductive layer after removing the portion of the conductive seed layer by using the conductive layer as part of a second electroplating process.
16. The method of claim 15, further comprising forming copper posts disposed between the semiconductor die and the conductive layer.
17. The method of claim 15, wherein forming the conductive layer further comprises:

forming a first portion of the conductive layer as a ground pad exposed within a footprint of the semiconductor die;

forming a second portion of the conductive layer as bussing lines disposed in the saw streets;

forming a third portion of the conductive layer as a contact pad coupled to the interconnect structure; and

forming a fourth portion of the conductive layer as a redistribution layer coupled to the semiconductor die and the contact pad.

18. The method of claim 17, further comprising:

forming the first, second, third, and fourth portions of the conductive layer as being electrically common; and

removing the bussing lines disposed in the saw streets such that portions of the conductive layer are no longer electrically common.

19. The method of claim 14, further comprising forming the interconnect structure using a plating jig.

20. The method of claim 14, further comprising forming the conductive layer using adaptive patterning to align the conductive layer with a true position of the semiconductor die.

CLAIMS

1. A method of making a plurality of fan-out wafer level packages (FOWLPs),
comprising:

providing an embedded die panel comprising a plurality of semiconductor die separated
by saw streets formed of encapsulant;

forming a planar conductive layer by an electroplating process, the planar conductive
layer comprising:

planar bussing lines disposed in the saw streets, and

a planar redistribution layer (RDL) formed at a same level as an entirety of the
planar bussing lines, the planar RDL being coupled to each of the plurality of semiconductor
die and the planar bussing lines;

forming an insulating layer over the planar conductive layer and the embedded die
panel that comprises openings disposed over the planar conductive layer outside a footprint of
each of the plurality of semiconductor die;

forming interconnect structures in the openings in the insulating layer by using the
planar conductive layer as a base layer during an electroplating process; and

singulating the embedded die panel through the saw streets after forming the
interconnect structures, wherein singulating removes at least a portion of the planar bussing
lines and forms the plurality of FOWLPs, wherein each of the plurality of FOWLPs comprises
a portion of the planar RDL vertically disposed between a contact pad of one of the plurality of
semiconductor die and one of the interconnect structures.

2. The method of claim 1, further comprising forming the embedded die panel by:
providing a carrier;
mounting the plurality of semiconductor die over the carrier; and
disposing an encapsulant around each of the plurality of semiconductor die and around a plurality of copper posts, wherein each of the plurality of semiconductor die is coupled to at least one copper post from the plurality of copper posts.
3. The method of claim 1, further comprising:
forming the planar conductive layer with a first thickness; and
forming the interconnect structures with a second thickness greater than the first thickness.
4. The method of claim 1, further comprising forming the FOWLPs comprising a thickness less than or equal to 0.6 millimeters.
5. The method of claim 1, further comprising forming the interconnect structures with a plating jig or a cover plate.
6. The method of claim 1, further comprising forming the planar conductive layer with adaptive patterning to align the planar conductive layer with a true position of the plurality of semiconductor die.

7. A method of making a plurality of fan-out wafer level packages (FOWLPs), comprising:

providing an embedded die panel comprising a plurality of semiconductor die separated by saw streets formed of encapsulant;

forming a planar conductive layer over the embedded die panel that extends from each of the plurality of semiconductor die into the saw streets, the planar conductive layer comprising:

bussing lines, and

an RDL formed at a same level as the bussing lines;

forming an insulating layer over the planar conductive layer and over the embedded die panel to comprise openings disposed over the planar conductive layer outside a footprint of each of the plurality of semiconductor die;

forming interconnect structures in the openings in the insulating layer by using the planar conductive layer as a base layer during a plating process; and

singulating the embedded die panel through the saw streets to remove a portion of the planar conductive layer in the saw streets and form the plurality of FOWLPs, wherein each of the plurality of FOWLPs comprises a portion of the RDL vertically disposed between a contact pad of one of the plurality of semiconductor die and one of the interconnect structures.

8. The method of claim 7, further comprising forming a ground pad over the planar conductive layer, the ground pad being exposed at an outer surface of the semiconductor device and at least partially overlapping one of the plurality of semiconductor die.

9. The method of claim 7, further comprising:
- forming a conductive seed layer over the embedded die panel;
- forming the planar conductive layer as a conductive pattern layer over the seed layer on the embedded die panel that extends from each of the plurality of semiconductor die into the saw streets; and
- removing the exposed conductive seed layer from the embedded die panel.
10. The method of claim 7, further comprising forming a copper post disposed between each of the plurality of semiconductor die and the planar conductive layer.
11. The method of claim 7, further comprising forming the interconnect structures with a plating jig or a cover plate.
12. The method of claim 7, further comprising forming the planar conductive layer with adaptive patterning to align the planar conductive layer with a true position of the plurality of semiconductor die.
13. The method of claim 9, further comprising forming the insulating layer to comprise openings disposed over the planar conductive layer inside a footprint of each of the plurality of semiconductor die.

14. A method of making a plurality of fan-out wafer level packages (FOWLPs), comprising:

providing a semiconductor die surrounded by saw streets;

forming a planar conductive layer that extends from over the semiconductor die into the saw streets;

forming an interconnect structure on the planar conductive layer; and

removing a portion of the planar conductive layer from the saw streets to form the plurality of fan-out wafer level packages.

15. The method of claim 14, further comprising:

forming the planar conductive layer over a conductive seed layer by a first electroplating process;

removing a portion of the conductive seed layer; and

forming the interconnect structure on the planar conductive layer after removing the portion of the conductive seed layer by using the planar conductive layer as a base layer as part of a second electroplating process.

16. The method of claim 15, further comprising forming a copper post disposed between the semiconductor die and the planar conductive layer.

17. The method of claim 15, wherein forming the planar conductive layer further comprises:

forming a first portion of the planar conductive layer as a ground pad exposed within a footprint of the semiconductor die;

forming a second portion of the planar conductive layer as bussing lines disposed in the saw streets;

forming a third portion of the planar conductive layer as a contact pad coupled to the interconnect structure; and

forming a fourth portion of the planar conductive layer as a redistribution layer coupled to the semiconductor die and the contact pad.

18. The method of claim 17, further comprising:

forming the first, second, third, and fourth portions of the planar conductive layer as being electrically common; and

removing the bussing lines disposed in the saw streets such that portions of the planar conductive layer are no longer electrically common.

19. The method of claim 14, further comprising forming the interconnect structure with a plating jig.

20. The method of claim 14, further comprising forming the planar conductive layer with adaptive patterning to align the planar conductive layer with a true position of the semiconductor die.