[0010] Furthermore, in Patent Document 4, to prevent the slack after expansion from causing it to become difficult to maintain the space between chips stably, a method of maintaining space between the chips (hereinafter referred to as the "kerf width" by shrinking the tape after the cutting process has been proposed.

RELATED ART

Patent Documents

[0011] Patent Document 1: JP2007-A-5530

Patent Document 2: JP2003-A-338467

Patent Document 3: JP2004-A-273895

Patent Document 4: JP2011-A-216508

SUMMARY

[0012] On the other hand, there was a problem in that when the thermal shrinkage stress during thermal shrinkage was large, the tape tends to expand more than the kerf width expanded in the expand process, and thus, the kerf width in the direction with the larger thermal shrinkage stress tends to expand more than necessary. Hence, the kerf width of the direction with the smaller thermal shrinkage stress often became narrower. By having a narrow kerf width, pickup defects occur. More specifically, when the value of the thermal shrinkage rate in the lengthwise direction divided by the thermal shrinkage rate in the widthwise direction is large, the difference between the lengthwise and widthwise directions become excessively large, and the kerf width becomes uneven, causing chip position displacement to occur, which leads to recognition defects during pickup. Further, when the kerf width is too narrow, re-adhering of the adhesive film occurs, causing pickup defects to occur. Note that the kerf width will not become even, even when the value of the thermal shrinkage rate in the lengthwise direction divided by the thermal shrinkage rate in the widthwise direction is a negative value.

[0013] Embodiments of the present invention seek to provide a semiconductor processing tape that

shows low thermal shrinkage rate and shrinks evenly regardless of the direction of the tape so that kerf width extends evenly without wrinkles or displacement in chip position occurring.

[0014] According to an aspect of the present invention, there is provided a semiconductor processing tape, wherein a thermal shrinkage rate in a lengthwise direction and a thermal shrinkage rate in a widthwise direction of the semiconductor processing tape are 0% or more to 20% or less when the semiconductor processing tape is heated at 100 ^{o}C for 10 seconds, and either one of the thermal shrinkage rate in the lengthwise direction or the thermal shrinkage rate in the widthwise direction is 7% or more, and a ratio of the thermal shrinkage rate in the lengthwise direction to the thermal shrinkage rate in the widthwise direction is 0.01 or more to 100 or less
(Note that in the equation, thermal shrinkage rate = (size before heating – size after heating)/size before heating x 100(%).),wherein the thermal shrinkage rate is obtained according to a method specified by JIS7162, in which a test sample of the tape is subjected to an extension distortion of 20 % at a rate of 500 mm/min and maintained for 60 seconds, after which the test sample is removed from the test equipment and heated at 100 ^{o}C for 10 seconds, and the thermal shrinkage rate before and after heating are measured.

[0015] Furthermore, the semiconductor processing tape is characterized in that in that it is utilized in a method for producing a semiconductor device, and the method includes following processes.

(a) a process of adhering a surface protection tape on a front side of a wafer on which a circuit pattern has been formed;

(b) a backgrinding process of grinding a back side of the wafer;

(c) a process of adhering an adhesive layer of the semiconductor processing tape on the back side of the wafer, while heating the wafer;

(d) a process of peeling the surface protection tape from the front side of the wafer;

(e) a process of forming a modified region within the wafer through multiple-photon absorption by irradiating laser to a predetermined division part on the wafer;

(f) an expand process of obtaining a plurality of chips with the adhesive layer attached thereto, by expanding the semiconductor processing tape to thereby divide the wafer and the adhesive layer of the semiconductor processing tape at a division line;

(g) a process of maintaining space between the chips, by heat-shrinking a part of the expanded semiconductor processing tape that does not overlap with the chips, to thereby remove a slack that occurs during the expand process; and

(h) a pickup process of picking up the chip with the adhesive layer attached thereto from the pressure-sensitive adhesive layer of the semiconductor processing tape.

from the pressure-sensitive adhesive layer of the semiconductor processing tape.

[0019] Further, the semiconductor processing tape is characterized in that in that it is utilized in a method for producing a semiconductor device, and the method includes following processes.

(a) a process of adhering a surface protection tape on a front side of a wafer on which a circuit pattern has been formed;

(b) a process of forming a modified region within the wafer through multiple-photon absorption by irradiating laser to a predetermined division part on the wafer;

(c) a backgrinding process of grinding a back side of the wafer;

(d) a process of adhering an adhesive layer of the semiconductor processing tape on the back side of the wafer, while heating the wafer;

(e) a process of peeling the surface protection tape from the front side of the wafer;

(f) an expand process of obtaining a plurality of chips with the adhesive layer attached thereto, by expanding the semiconductor processing tape to thereby divide the wafer and the adhesive layer of the semiconductor processing tape along a division line;

(g) a process of maintaining space between the chips, by heat-shrinking a part of the expanded semiconductor processing tape that does not overlap with the chips, to thereby remove a slack that occurs during the expand process; and

(h) a pickup process of picking up the chip with the adhesive layer attached thereto from the pressure-sensitive adhesive layer of the semiconductor processing tape.

[0020] Further, there is disclosed a semiconductor processing tape, wherein either the thermal shrinkage rate of the semiconductor processing tape in either the lengthwise direction or the widthwise direction is 0.1 % or more.

Furthermore, the present invention relates to a semiconductor device that utilizes the semiconductor processing tape.

Effect of the Invention

[0021] By using the semiconductor processing tape provided by embodiments of the present invention, the even expansion without change in the kerf width is made possible, and thus, a highly reliable semiconductor device so that the chip position does not deviate

Claims

1. A semiconductor processing tape, a thermal shrinkage rate in a lengthwise direction and a thermal shrinkage rate in a widthwise direction of the semiconductor processing tape are 0% or more and 20% or less when the semiconductor processing tape is heated at 100 ^{o}C for 10 seconds, and either one of the thermal shrinkage rate in the lengthwise direction or the thermal shrinkage rate in the widthwise direction is 7% or more, and a ratio of the thermal shrinkage rate in the lengthwise direction to the thermal shrinkage rate in the widthwise direction is 0.01 or more and 100 or less, wherein the thermal shrinkage rate is obtained from an equation the thermal shrinkage rate(%) = (size before heating – size after heating) / size before heating x 100, wherein the thermal shrinkage rate is obtained according to a method specified by JIS7162, in which a test sample of the tape is subjected to an extension distortion of 20 % at a rate of 500 mm/min and maintained for 60 seconds, after which the test sample is removed from the test equipment and heated at 100 ^{o}C for 10 seconds, and the thermal shrinkage rate before and after heating are measured.

2. The semiconductor processing tape according to claim 1, wherein the semiconductor processing tape is utilized in a method for producing a semiconductor device, the method comprises:

(a) a process of adhering a surface protection tape on a front side of a wafer on which a circuit pattern has been formed;

(b) a backgrinding process of grinding a back side of the wafer;

(c) a process of adhering an adhesive layer of the semiconductor processing tape on the back side of the wafer, while heating the wafer;

(d) a process of peeling the surface protection tape from the front side of the wafer;

(e) a process of forming a modified region within the wafer through multiple-photon absorption by irradiating laser to a predetermined division part on the wafer;

(f) an expand process of obtaining a plurality of chips with the adhesive layer attached thereto, by expanding the semiconductor processing tape to thereby divide the wafer and the adhesive layer of the semiconductor processing tape at a division line;

(g) a process of maintaining space between the chips, by heat-shrinking a part of the expanded semiconductor processing tape that does not overlap with the chips, to thereby remove a slack that occurs during the expand process; and

(h) a pickup process of picking up the chip with the adhesive layer attached thereto

(g) a process of maintaining space between the chips by heat-shrinking a part of the expanded semiconductor processing tape that does not overlap with the chips, to thereby remove a slack that occurs during the expand process; and

(h) a pickup process of picking up the chip with the adhesive layer attached thereto from the pressure-sensitive adhesive layer of the semiconductor processing tape.

6. The semiconductor processing tape according to claim 1, wherein the semiconductor processing tape is utilized in a method for producing a semiconductor device, the method comprises:

(a) a process of adhering a surface protection tape on a front side of a wafer on which a circuit pattern has been formed;

(b) a process of forming a modified region within the wafer through multiple-photon absorption by irradiating laser to a predetermined division part on the wafer;

(c) a backgrinding process of grinding a back side of the wafer;

(d) a process of adhering an adhesive layer of the semiconductor processing tape on the back side of the wafer, while heating the wafer;

(e) a process of peeling the surface protection tape from the front side of the wafer;

(f) an expand process of obtaining a plurality of chips with the adhesive layer attached thereto, by expanding the semiconductor processing tape to thereby divide the wafer and the adhesive layer of the semiconductor processing tape along a division line;

(g) a process of maintaining space between the chips, by heat-shrinking a part of the expanded semiconductor processing tape that does not overlap with the chips, to thereby remove a slack that occurs during the expand process; and

(h) a pickup process of picking up the chip with the adhesive layer attached thereto from the pressure-sensitive adhesive layer of the semiconductor processing tape.

7. A semiconductor device that utilizes the semiconductor processing tape according to any one of claims 1 to 6.