

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to networks that receive and transmit groups of logic signals from remote locations and, more particularly, to an apparatus for insuring the accuracy of the information transmitted between the local and the remote locations.

2. Description of the Related Art

In the Symposium Record of the 1987 IEEE International Symposium on Electromagnetic Compatibility, 15-27.08.1987, page 290-296, Atlanta, Georgia, A. Partyka describes a Fault-Tolerant Bus Transceiver System with means for eliminating jamming and RF interference. The system includes a multiloop structure in which each element is periodically and automatically tested and in which failure of any single component does not result in uncontrolled carrier transmission. The system allows for isolation and reporting of any single element failure before fatal multiple failure can occur. The system includes means and method steps as described in the preamble of the independent claims. Each time the microprocessor wants to send data, it has to perform certain relatively complex operations of toggling the two or more input signals of a sequencer, whose output is active in one and only one state. In the simplest version the sequencer can be just a counter. Acting more intelligently, the processor can make the sequencer to reach the state number N-1. Then only one change of the processor output port can activate the RF switch, and the next one would already deactivate it. The key idea is that the processor can access the RF switch only if it acts intelligently, precisely according to the program. Any random inputs to the sequencer are neglected. An additional level of security can be added by coupling the action of the sequencer with the action of two timers of which the first one is activated by the sequencer output. When a prescribed time elapses and the output of the sequencer is still active, this timer resets the sequencer, thus even if the processor fails to change the sequencer state after transmitting a message, the RF switch is still turned off. Whenever a processor malfunction is detected either by a processor activity detector or by the first mentioned timer, then the second timer is activated and power is disconnected from the amplifier for a relatively long time by means of a supply voltage switch.

In the automatic control of processes, process control networks are provided to collect status information by at least one central location and to distribute control signals to the devices coupled to the network. Referring to Fig. 1, a portion of such a process

control network is shown. The process control network includes a system bus 5 which has at least one central control unit 6 coupled thereto and at least one bus interface module 9 also coupled thereto. The central control unit 6 receives signals from the system bus 5 that typically communicate the status of user devices coupled to the process control network and applies signals to the network that provide the control signals determining the operation of the user devices. The bus interface unit 9 applies status signals to the system bus and receives signals from the system bus 5 which are relevant to a subset of network user devices 10 that communicate with the central control unit 6 through bus interface unit 9. User devices 10 responding to digital signals, such as motors, lamps and heaters, receive control signals through device interface unit 16 and digital output module 12 from the bus interface unit 9. User devices 10 providing digital status signals in response to contact closures provide status signals to the bus interface unit 9 by means of device interface unit 17 and digital input module 13. User devices 10 responding to analog control signals, such as control valves, receive signals from the bus interface unit 9 by means of output analog module 14 and device interface unit 18. User devices 10 of the type providing analog status information such as flowmeters, level detectors, pressure meters etc. provide the status signals to the bus interface unit through interface module 19 and analog input module 15. The device interface units 16, 17, 18 and 19 convert the signals received from and transmitted to the user devices into a format usable by the digital output and input modules and the analog output and input modules, respectively. The digital input and output modules 13 and 12 and the analog input and output modules 15 and 14 couple the signals of the user devices, as transformed by the device interface unit, with the bus interface unit 9 by means of local bus 11.

In the communication between the bus interface unit 9 and the digital and analog input and output devices, the messages typically have an upper bound on the time that a single message can be active (In the preferred embodiment, the upper limit is 10 milliseconds [ms]), however, this interval is a matter of design choice. A malfunction in the network can result in uncontrolled communication of information, generally referred to as jabber, in which the message can extend beyond the 10 ms boundary. Because the jabber is the result of a malfunction, such a condition must be detected and the network repaired or inactivated. The detection of a jabber event is typically performed by an antijabber timing unit which measures the length of the message. However, the antijabber circuit can itself malfunction and not detect a jabbering incident. Furthermore, in process control networks of the related art, a jabber incident can be the result of a single component malfunction.

A need has therefore been felt for apparatus and

method that can verify the operation of the antijabber timing circuit without comprising the normal communication operation and which can assist in isolating a malfunction that could result in a jabber event, the jabber event resulting in interruption of communication on the network beyond the immediate consequence of the malfunction.

It is an object of the present invention to provide an improved process control network and an improved method for the exchange of signals on a process control network wherein failure of a single component in the associated process control network does not result in a jabber event.

These objects are achieved by the invention as described in the independent claims.

The invention further discloses a process control network having an antijabber circuit and having the capability of testing an antijabber timing circuit. Preferred details of the new method and embodiments of the new apparatus are described in the dependent claims.

SUMMARY OF THE INVENTION

The aforementioned and other features are accomplished according to the present invention, by providing a microprocessor unit with the capability of applying a timing signal to the antijabber timing unit. The timing signal has a duration longer than the maximum permitted message duration. When the antijabber circuit is functioning properly, a failure signal is transmitted to the microprocessor. In the event of a malfunction in the antijabber circuit, the microprocessor will detect that no failure signal was received as a result of the timing signal and appropriate response can be taken. A signal is applied to the properly functioning antijabber to remove the failure signal and apparatus is provided to insure that the removal of the failure signal does not compromise the network communication. The antijabber circuit is also used to supply a second enable signal for the network to minimize the opportunity for a single component to result in a jabber event.

These and other features of the present invention will be understood upon reading of the following description along with the drawings.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1 is a block diagram of process control network capable of using the present invention.

Figure 2 is a block diagram of the principal components of the apparatus for testing an antijabber timing unit.

Figure 3 is a timing diagram illustrating the relationship of the important signals used for testing the antijabber timing unit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

1. Detailed Description of the Figures

Fig. 1 has been described with reference to the related art.

Referring now to Fig. 2, the apparatus for testing the antijabber circuit is illustrated. Logic signal groups are exchanged between the microprocessor unit 21 and the communication channel transceivers 22 and 23 when the communications channel transceivers 22 or 23 are enabled. The microprocessor unit 21 applies an UNLOCK signal to antijabber timing unit 24 and to a second input terminal of logic 'AND' gate 25 and applies a REQUEST signal to the antijabber timing unit 24 and to a first terminal of logic 'AND' gate 27, to a first input terminal of logic 'AND' gate 26 and to a first terminal of logic 'AND' gate 25. The microprocessor receives a LOCKED-UP signal from antijabber timing unit 24 and a RESET signal from an output terminal of logic 'AND' gate 25. An output window signal from antijabber timing unit 24 is applied to a second input terminal of logic 'AND' gate 27 and to a second input terminal of logic 'AND' gate 26. The logic 'AND' gate 27 applies an ENABLE signal to communication channel transceiver 22 and logic 'AND' gate 26 applies an ENABLE signal to communication channel transceiver 23. Communication channel transceivers 22 and 23 exchange signal groups with the remainder of the process control network.

Referring next to Fig. 3, the relationship of principal signals of the preferred embodiment are shown. A timing or REQUEST signal is generated by the microprocessor unit 21 and applied to antijabber timing unit 24. After a period of time that exceeds the maximum period permitted for a message, the antijabber timing unit provides a LOCKED-UP signal indicating that the antijabber timing unit has detected a message that exceeds the maximum permitted length. In response to the LOCKED-UP signal, applied to the microprocessor, the microprocessor applies an UNLOCK signal to the antijabber timing unit 24. Although the original REQUEST signal is inactivated prior to generation of the UNLOCK signal, a current REQUEST signal related to an actual message transmission can be present. The combination of a REQUEST signal and an UNLOCK signal causes the microprocessor to be reset by a RESET signal regardless of the state of the LOCKED-UP signal.

2. Operation of the Preferred Embodiment

The present invention makes use of the processing capability of a microprocessor unit used for transmission of messages over the network to provide a timing signal and determine if, as a result of the timing

signal, the antijabber timing unit functioned correctly.. Because the timing signal exceeds the maximum permitted message length, if a LOCKED-UP (failure) signal is not generated as a result of the timing signal, then the microprocessor unit responds to an antijabber timing unit malfunction. When a LOCKED-UP signal is generated by the antijabber timing unit, the microprocessor responds with an UNLOCK signal to the antijabber unit that inactivates the LOCKED-UP signal. Because the timing signal has been removed, a message request signal can be applied to the antijabber unit. To prevent the UNLOCK signal from impacting the operation of a message transmission, the simultaneous presence of an UNLOCK signal and a message request signal results in the resetting of the microprocessor unit, i.e., any activity in progress will be aborted and reinitiated.

Referring once again to Fig. 2, an important feature of the present invention is illustrated. The ENABLE signal for the communication channel transceiver 22 from logic 'AND' gate 27 and the ENABLE signal for the communication channel transceiver 23 from logic 'AND' gate 26 are activated by two signals, one from the microprocessor unit 21 and one (the WINDOW signal) from the antijabber timing unit. Thus, a component malfunction that would normally result in a jabber incident is prevented from so doing because of the presence of the second activation component. The WINDOW signal is present when the LOCKED-UP signal is not present, when a REQUEST signal is present and when the REQUEST signal has been active for less than the maximum signal transmission time.

It will be clear that, although the preferred embodiment uses the processing capability of a microprocessor unit, the same antijabber timing unit testing can be performed by dedicated apparatus.

The foregoing description is included to illustrate the operation of the preferred embodiment and is not meant to limit the scope of the invention. The scope of the invention is to be limited only by the following claims.

Claims

1. Apparatus for preventing uncontrolled communication in a communication network (22, 23) comprising:

- a) a first unit (21) for generating a first signal (REQUEST), which first signal normally denotes the transmission of data signals in said network;
- b) a second unit (24) including a timing element coupled to said first unit for receiving said first signal, said second unit responsive to said first signal, and when operating correctly, generating a second signal (LOCKED

UP) if said first signal exceeds a predetermined duration; characterized by

- c) means for coupling said second signal to said first unit (21) to provide notification to said first unit (21) that said first signal exceeded said predetermined duration;
- d) said first unit (21) including means responding to said second signal to generate a third signal (UNLOCK) and to apply said third signal to said second unit (24); and
- e) said second unit (24) including means responding to said third signal to terminate said second signal (LOCKED UP).

2. The apparatus of claim 1, characterized by :

- a) said first unit (21) being a microprocessor and said second unit (24) being an anti-jabber timing unit;
- b) said microprocessor (21) including means for generating said first signal also during a test procedure;
- c) means responsive to said second signal (LOCKED UP) for preventing transmission of data signals by said microprocessor (21) and for causing said microprocessor to apply said third signal (UNLOCK) to said anti-jabber timing unit (24) after said first signal (REQUEST) is removed during said test procedure, whereat said third signal (UNLOCK) causes said anti-jabber timing unit (24) to cancel said second signal (LOCKED UP); and
- d) means within said microprocessor (21) for preventing transmission of data signals when said second signal (LOCKED UP) is not generated during said test procedure.

3. The apparatus of claim 2, characterized by

- a) a logic gate (25) responsive to a simultaneous presence of said third signal (UNLOCK) and said first signal (REQUEST) for providing a fourth signal (RESET); and
- b) means for applying said fourth signal to said microprocessor (21) and for causing said microprocessor to halt operation and to be reset.

4. The apparatus of one of the preceding claims, characterized by isolating means (26, 27) provided between said first (21) and second (24) unit on the one hand and said communication network (22, 23) on the other hand for reducing effects of single component failure on transmission of data signals over said communication network by providing a plurality of enabling signals for each of a plurality of communication channels (22, 23).

5. The apparatus of claim 4, characterized in that



signal, the antijabber timing unit functioned correctly.. Because the timing signal exceeds the maximum permitted message length, if a LOCKED-UP (failure) signal is not generated as a result of the timing signal, then the microprocessor unit responds to a antijabber timing unit malfunction. When a LOCKED-UP signal is generated by the antijabber timing unit, the microprocessor responds with an UNLOCK signal to the antijabber unit that inactivates the LOCKED-UP signal. Because the timing signal has been removed, a message request signal can be applied to the antijabber unit. To prevent the UNLOCK signal from impacting the operation of a message transmission, the simultaneous presence of an UNLOCK signal and a message request signal results in the resetting of the microprocessor unit, i.e., any activity in progress will be aborted and reinitiated.

Referring once again to Fig. 2, an important feature of the present invention is illustrated. The ENABLE signal for the communication channel transceiver 22 from logic 'AND' gate 27 and the ENABLE signal for the communication channel transceiver 23 from logic 'AND' gate 26 are activated by two signals, one from the microprocessor unit 21 and one (the WINDOW signal) from the antijabber timing unit. Thus, a component malfunction that would normally result in a jabber incident is prevented from so doing because of the presence of the second activation component. The WINDOW signal is present when the LOCKED-UP signal is not present, when a REQUEST signal is present and when the REQUEST signal has been active for less than the maximum signal transmission time.

It will be clear that, although the preferred embodiment uses the processing capability of a microprocessor unit, the same antijabber timing unit testing can be performed by dedicated apparatus.

The foregoing description is included to illustrate the operation of the preferred embodiment and is not meant to limit the scope of the invention. The scope of the invention is to be limited only by the following claims.

Claims

1. Apparatus for preventing uncontrolled communication in a communication network (22, 23) comprising:
 - a) a first unit (21) for generating a first signal (REQUEST), which first signal normally denotes the transmission of data signals in said network;
 - b) a second unit (24) including a timing element coupled to said first unit for receiving said first signal, said second unit responsive to said first signal, and when operating correctly, generating a second signal (LOCKED UP) if said first signal exceeds a predetermined duration; characterized by
 - c) means for coupling said second signal to said first unit (21) to provide notification to said first unit (21) that said first signal exceeded said predetermined duration;
 - d) said first unit (21) including means responding to said second signal to generate a third signal (UNLOCK) and to apply said third signal to said second unit (24); and
 - e) said second unit (24) including means responding to said third signal to terminate said second signal (LOCKED UP).
2. The apparatus of claim 1, characterized by :
 - a) said first unit (21) being a microprocessor and said second unit (24) being an anti-jabber timing unit;
 - b) said microprocessor (21) including means for generating said first signal also during a test procedure;
 - c) means responsive to said second signal (LOCKED UP) for preventing transmission of data signals by said microprocessor (21) and for causing said microprocessor to apply said third signal (UNLOCK) to said anti-jabber timing unit (24) after said first signal (REQUEST) is removed during said test procedure, whereat said third signal (UNLOCK) causes said anti-jabber timing unit (24) to cancel said second signal (LOCKED UP); and
 - d) means within said microprocessor (21) for preventing transmission of data signals when said second signal (LOCKED UP) is not generated during said test procedure.
3. The apparatus of claim 2, characterized by
 - a) a logic gate (25) responsive to a simultaneous presence of said third signal (UNLOCK) and said first signal (REQUEST) for providing a fourth signal (RESET); and
 - b) means for applying said fourth signal to said microprocessor (21) and for causing said microprocessor to halt operation and to be reset.
4. The apparatus of one of the preceding claims, characterized by isolating means (26, 27) provided between said first (21) and second (24) unit on the one hand and said communication network (22, 23) on the other hand for reducing effects of single component failure on transmission of data signals over said communication network by providing a plurality of enabling signals for each of a plurality of communication channels (22, 23).
5. The apparatus of claim 4, characterized in that



said anti-jabber timing unit (24) includes signal means for generating a fifth signal (WINDOW) when said second signal (LOCKED UP) is not present, wherein said first signal (REQUEST) and said fifth signal (WINDOW) enable communication from said microprocessor (21) to said communication network (22, 23).

6. The apparatus of one of the preceding claims, characterized by testing means for verifying operation of said anti-jabber timing unit (24), said testing means including first means in said microprocessor (21) for generating said first signal (REQUEST) longer than said predetermined length of time during a test procedure, wherein said anti-jabber timing unit (24) is adapted to provide said second signal (LOCKED UP) after said predetermined length of time; and by said microprocessor (21) including second means for identifying an anti-jabber timing unit malfunction when said second signal (LOCKED UP) is not generated during said test procedure.

7. A method for preventing uncontrolled communication over a communication network, comprising the steps of:

- a) generating a first signal (REQUEST) when a microprocessor (21) transmits data signals to said communication network (22, 23);
- b) applying said first signal (REQUEST) to a timing unit (24); and
- c) generating a second signal (LOCKED UP) by said timing unit (24) when said first signal (REQUEST) associated with said data signals exceeds a predetermined period; characterized by the further steps of:
- d) applying said second signal (LOCKED UP) to said microprocessor (21), said second signal identifying a jabber event;
- e) periodically generating a test first signal (REQUEST) exceeding said predetermined period, said test first signal (REQUEST) being applied to said timing unit (24);
- f) generating a third signal (UNLOCK) by said microprocessor (21) when a second signal is received in response to said test first signal and applying said third signal to said timing unit (24), wherein said second signal is removed in response to said third signal; and
- g) preventing transmission of data signals to said communication network by said microprocessor (21) when said second signal (LOCKED UP) is not generated in response to said test first signal (REQUEST).

8. The method of claim 7, characterized by the further step of reinitiating transmission of data sig-

nals by said microprocessor (21) when said test first signal (REQUEST) and said third signal (UNLOCK) are simultaneously present.

9. The method of claim 7 or 8, characterized by the further step of generating a fifth signal (WINDOW) by said timing unit (24) when said second signal (LOCKED UP) is not present, said fifth signal (WINDOW) providing a separate signal for enabling transmission of data signals to said communication network.
10. The method of claim 7, 8 or 9, characterized in that said first signal (REQUEST) is an activation signal for permitting data signals to be transmitted to said communications network (22, 23).

Patentansprüche

1. Einrichtung zum Verhindern unkontrollierter Kommunikation in einem Kommunikationsnetzwerk (22, 23) mit

a) einer ersten Einheit (21) zum Erzeugen eines ersten Signals (ANFORDERUNG), welches normalerweise die Übertragung von Datensignalen im Netzwerk bezeichnet;

b) einer zweiten Einrichtung (24) mit einem an die erste Einheit angeschlossenen Zeitgeber zum Empfang des ersten Signals, welche auf das erste Signal anspricht und bei ordnungsgemäßem Betrieb ein zweites Signal (SPERRUNG) erzeugt, sobald das erste Signal eine vorgegebene Dauer überschreitet;

gekennzeichnet durch

c) Mittel zum Ankoppeln des zweiten Signals an die erste Einheit (21), um dieser mitzuteilen, daß das erste Signal die vorgegebene Zeitdauer überschreitet;

d) auf das zweite Signal ansprechende Mittel in der ersten Einheit (21), um ein drittes Signal (ENTSPERRUNG) zu erzeugen und der zweiten Einheit (24) zuzuführen; und

e) auf das dritte Signal ansprechende Mittel in der zweiten Einheit (24), um das zweite Signal (SPERRUNG) zu beenden.

2. Einrichtung nach Anspruch 1, gekennzeichnet durch

a) die Ausbildung der ersten Einheit (21) als Mikroprozessor und der zweiten Einheit (24) als Antiverwaschungs-Zeitgeber;

b) Mittel im Mikroprozessor (21) zur Erzeugung des ersten Signals auch während eines Testvorgangs;

c) auf das zweite Signal (SPERRUNG) ansprechende Mittel zum Verhindern der Übertragung von Datensignalen durch den Mikro-



- prozessor (21) und zur Zufuhr des dritten Signals (ENTSPERRUNG) durch den Mikroprozessor an die Antiverwaschungs-Zeitgebereinheit (24), nachdem das erste Signal (ANFORDERUNG) während des Testvorgangs entfernt wurde, wobei das dritte Signal (ENTSPERRUNG) die Antiverwaschungs-Zeitgebereinheit (24) veranlaßt, das zweite Signal (SPERRUNG) zu beseitigen; und
- d) Mittel innerhalb des Mikroprozessors (21) zum Verhindern der Übertragung von Datensignalen, wenn das zweite Signal (SPERRUNG) nicht während des Testvorgangs erzeugt wird.
3. Einrichtung nach Anspruch 2, gekennzeichnet durch
- a) ein auf eine gleichzeitige Anwesenheit des dritten Signals (ENTSPERRUNG) und des ersten Signals (ANFORDERUNG) ansprechendes Logikgatter (25) zur Erzeugung eines vierten Signals (RÜCKSTELLUNG); und
- b) Mittel zur Zufuhr des vierten Signals an den Mikroprozessor (21) sowie zum Anhalten des Betriebs des Mikroprozessors und zur Rücksetzung.
4. Einrichtung nach einem der vorangehenden Ansprüche, gekennzeichnet durch zwischen den ersten (21) und zweiten (24) Einheiten einerseits und dem Kommunikationsnetzwerk (22, 23) andererseits angeordnete Isolierschaltungen (26, 27) zur Verringerung der Auswirkung eines Einzelkomponentenfehlers auf die Übertragung von Datensignalen über das Kommunikationsnetzwerk, in dem für jeden von mehreren Übertragungskanälen (22, 23) mehrere Aktivierungssignale erzeugt werden.
5. Einrichtung nach Anspruch 4, dadurch gekennzeichnet, daß die Antiverwaschungs-Zeitgebereinheit (24) zwei Signaleinrichtungen zur Erzeugung eines fünften Signals (FENSTER) umfaßt, wenn das zweite Signal (SPERRUNG) nicht ansteht, und wobei das erste Signal (ANFORDERUNG) sowie das fünfte Signal (FENSTER) die Kommunikation vom Mikroprozessor (21) zum Kommunikationsnetzwerk (22, 23) aktivieren.
6. Einrichtung nach einem der vorangehenden Ansprüche, gekennzeichnet durch eine Testeinrichtung zum Verifizieren des Betriebs der Antiverwaschungs-Zeitgebereinheit (24), wobei die Testeinrichtung erste Mittel innerhalb des Mikroprozessors (21) zum Erzeugen des ersten Signals (ANFORDERUNG) für eine Zeitspanne länger als die vorgegebene Zeitspanne während des Testvorgangs umfaßt, und wobei die Antiverwaschungs-Zeitgebereinheit (24) das zweite Signal (SPERRUNG) nach Ablauf der vorgegebenen Zeitspanne liefert; und durch zweite Mittel im Mikroprozessor (21) zum Identifizieren einer Fehlfunktion der Antiverwaschungs-Zeitgebereinheit, falls das zweite Signal (SPERRUNG) nicht während des Testvorgangs erzeugt wird.
7. Verfahren zum Verhindern unkontrollierter Kommunikation über ein Kommunikationsnetzwerk mit den Schritten:
- a) Erzeugen eines ersten Signals (ANFORDERUNG), sobald ein Mikroprozessor (21) Datensignale an das Kommunikationsnetzwerk (22, 23) überträgt;
- b) Anlegen des ersten Signals (ANFORDERUNG) an eine Zeitgebereinheit; und
- c) Erzeugen eines zweiten Signals (SPERRUNG) durch die Zeitgebereinheit (24), wenn das den Datensignalen zugeordnete erste Signal (ANFORDERUNG) eine vorgegebene Zeitspanne überdauert;
- gekennzeichnet durch die weiteren Schritte:
- d) Anlegen des zweiten Signals (SPERRUNG) an den Mikroprozessor, wobei das zweite Signal einen Verwaschungsvorgang anzeigt;
- e) periodisches Erzeugen eines ersten Testsignals (ANFORDERUNG), welches die vorgegebene Zeitspanne übersteigt und welches der Zeitgebereinheit (24) zugeleitet wird;
- f) Erzeugen eines dritten Signals (ENTSPERRUNG) durch den Mikroprozessor (21), sobald ein zweites Signal als Antwort auf das erste Testsignal empfangen wird, sowie Zufuhr des dritten Signals an die Zeitgebereinheit, wobei das zweite Signal in Beantwortung des dritten Signals beseitigt wird; und
- g) Verhindern der Übertragung von Datensignalen durch den Mikroprozessor (21) an das Kommunikationsnetzwerk, wenn das zweite Signal (SPERRUNG) nicht in Beantwortung des ersten Testsignals (ANFORDERUNG) erzeugt wird.
8. Verfahren nach Anspruch 7, gekennzeichnet durch den weiteren Schritt einer Wiederaktivierung der Übertragung von Datensignalen durch den Mikroprozessor (21), wenn das erste Testsignal (ANFORDERUNG) und das dritte Signal (ENTSPERRUNG) gleichzeitig anstehen.
9. Verfahren nach Anspruch 7 oder 8, gekennzeichnet durch den weiteren Schritt der Erzeugung eines fünften Signals (FENSTER) durch die Zeitgebereinheit (24), sobald das zweite Signal (SPERRUNG) nicht vorhanden ist, und wobei das fünfte Signal (FENSTER) ein getrenntes Si-



gnal für die Aktivierung der Übertragung von Datensignalen an das Kommunikationsnetzwerk liefert.

10. Verfahren nach Anspruch 7, 8 oder 9, dadurch gekennzeichnet, daß das erste Signal (ANFORDERUNG) ein Aktivierungssignal für die Zulassung der Übertragung von Datensignalen an das Kommunikationsnetzwerk (22, 23) ist.

Revendications

1. Appareil destiné à empêcher une communication non contrôlée dans un réseau de communication (22, 23), comprenant:

- a) une première unité (21) pour générer un premier signal (REQUETE), lequel premier signal indique normalement l'émission de signaux de données dans ledit réseau;
- b) une seconde unité (24) comportant un élément de cadencement couplé à ladite première unité pour recevoir ledit premier signal, ladite seconde unité étant sensible audit premier signal et lorsqu'elle fonctionne correctement, elle génère un second signal (VERROUILLAGE) si ledit premier signal dépasse une durée prédéterminée, caractérisé par:
- c) un moyen destiné à coupler ledit second signal à ladite première unité (21) pour produire une notification pour ladite première unité (21) consistant en ce que ledit premier signal a dépassé ladite durée prédéterminée;
- d) ladite première unité (21) comportant un moyen sensible audit second signal pour générer un troisième signal (DEVERROUILLAGE) et pour appliquer ledit troisième signal à ladite seconde unité (24); et
- e) ladite seconde unité (24) comportant un moyen sensible audit troisième signal pour terminer ledit second signal (VERROUILLAGE).

2. Appareil selon la revendication 1, caractérisé en ce que:

- a) ladite première unité (21) est un microprocesseur et ladite seconde unité (24) est une unité de cadencement d'anti-émission continue;
- b) ledit microprocesseur (21) comporte un moyen pour générer ledit premier signal également pendant une procédure de test;
- c) un moyen sensible audit second signal (VERROUILLAGE) est prévu pour empêcher une émission de signaux de données par ledit microprocesseur (21) et pour forcer ledit microprocesseur à appliquer ledit troisième si-

gnal (DEVERROUILLAGE) à ladite unité de cadencement d'anti-émission continue (24) après que ledit premier signal (REQUETE) est ôté pendant ladite procédure de test, si bien que ledit troisième signal (DEVERROUILLAGE) force ladite unité de cadencement d'anti-émission continue (24) à annuler ledit second signal (VERROUILLAGE); et d) un moyen est prévu dans ledit microprocesseur (21) pour empêcher une émission de signaux de données lorsque ledit second signal (VERROUILLAGE) n'est pas généré pendant ladite procédure de test.

3. Appareil selon la revendication 2, caractérisé par:
- a) une porte logique (25) sensible à une présence simultanée dudit troisième signal (DEVERROUILLAGE) et dudit premier signal (REQUETE) pour produire un quatrième signal (REMISE A L'ETAT INITIAL); et
 - b) un moyen pour appliquer ledit quatrième signal audit microprocesseur (21) et pour forcer ledit microprocesseur à arrêter son fonctionnement et à être remis à l'état initial.

4. Appareil selon l'une quelconque des revendications précédentes, caractérisé par un moyen d'isolation (26, 27) prévu entre lesdites première (21) et seconde (24) unités d'une part et ledit réseau de communication (22, 23) d'autre part pour réduire des effets d'une défaillance de composant unique lors d'une émission de signaux de données sur ledit réseau de communication en prévoyant une pluralité de signaux de validation pour chacune d'une pluralité de canaux de communication (22, 23).

5. Appareil selon la revendication 4, caractérisé en ce que ladite unité de cadencement d'anti-émission continue (24) comporte un moyen de signal pour générer un cinquième signal (FENETRE) lorsque ledit second signal (VERROUILLAGE) n'est pas présent, dans lequel ledit premier signal (REQUETE) et ledit cinquième signal (FENETRE) permettent une communication depuis ledit microprocesseur (21) jusqu'audit réseau de communication (22, 23).

6. Appareil selon l'une quelconque des revendications précédentes, caractérisé par un moyen de test pour vérifier un fonctionnement de ladite unité de cadencement d'anti-émission continue (24), ledit moyen de test comportant un premier moyen prévu dans ledit microprocesseur (21) pour générer ledit premier signal (REQUETE) de manière à ce qu'il soit plus long que ladite longueur temporelle prédéterminée pendant une procédure de test, dans lequel ladite unité de cadencement



d'anti-émission continue (24) est conçue pour produire ledit second signal (VERROUILLAGE) après ladite durée temporelle prédéterminée;

et en ce que ledit microprocesseur (21) comporte un second moyen pour identifier un dysfonctionnement de l'unité de cadencement d'anti-émission continue lorsque le second signal (VERROUILLAGE) n'est pas généré pendant ladite procédure de test.

7. Procédé pour empêcher une communication non contrôlée sur un réseau de communication, comprenant les étapes de:

a) génération d'un premier signal (REQUETE) lorsqu'un microprocesseur (21) émet des signaux de données pour ledit réseau de communication (22, 23);

b) application dudit premier signal (REQUETE) à une unité de cadencement (24); et

c) génération d'un second signal (VERROUILLAGE) par ladite unité de cadencement (24) lorsque ledit premier signal (REQUETE) associé auxdits signaux de données dépasse une période prédéterminée;

caractérisé par les étapes supplémentaires de:

d) application dudit second signal (VERROUILLAGE) audit microprocesseur (21), ledit second signal identifiant un événement d'anti-émission continue;

e) génération périodique d'un premier signal de test (REQUETE) dépassant ladite période prédéterminée, ledit premier signal de test (REQUETE) étant appliqué à ladite unité de cadencement (24);

f) génération d'un troisième signal (DEVERROUILLAGE) par ledit microprocesseur (21) lorsqu'un second signal est reçu en réponse audit premier signal de test et application dudit troisième signal à ladite unité de cadencement (24), dans lequel ledit second signal est ôté en réponse audit troisième signal; et

g) empêchement d'une émission de signaux de données pour ledit réseau de communication par ledit microprocesseur (21) lorsque ledit second signal (VERROUILLAGE) n'est pas généré en réponse audit premier signal de test (REQUETE).

8. Procédé selon la revendication 7, caractérisé par l'étape supplémentaire de réinitialisation d'une émission de signaux de données par ledit microprocesseur (21) lorsque ledit premier signal de test (REQUETE) et ledit troisième signal (DEVERROUILLAGE) sont simultanément présents.

9. Procédé selon la revendication 7 ou 8, caractérisé

par l'étape supplémentaire de génération d'un cinquième signal (FENETRE) par ladite unité de cadencement (24) lorsque ledit second signal (VERROUILLAGE) n'est pas présent, ledit cinquième signal (FENETRE) constituant un signal distinct pour valider une émission de signaux de données sur ledit réseau de communication.

10. Procédé selon la revendication 7, 8 ou 9, caractérisé en ce que ledit premier signal (REQUETE) est un signal d'activation destiné à permettre l'émission de signaux de données sur ledit réseau de communication (22, 23).