ABSTRACT

PROCESSOR ORDERING CONSISTENCY FOR A PROCESSOR PERFORMING OUT-OF-ORDER INSTRUCTION EXECUTION

A method for processor ordering in a multiprocessor computer system, wherein a processor snoops a multiprocessor bus for an external store operation to the memory address of each executed and unretired load memory instruction. The processor commits the result data value of each executed and unretired load memory instruction to an architectural state in the sequential program order if the corresponding external store operation is not detected. The processor discards the result data value of the executed and unretired load memory instruction if the corresponding external store operation is detected. The processor then reexecutes the instruction stream starting at the load memory instruction causing the external store snoop detect.

(Fig. 2)