

**TRANSITION METAL DICHALCOGENIDES AND USES THEREOF****Cross Reference to Related Application(s)**

- 5     The present disclosure claims the benefit of Singapore Patent Application No. 10201906808T, which is incorporated in its entirety by reference herein.

**Technical Field**

- The present invention relates to transition metal dichalcogenides, particularly the use  
10    of transition metal dichalcogenides in electronic devices.

**Background**

- Two-dimensional (2D) transition metal dichalcogenides (TMDs) have been  
15    established as promising building blocks for the next-generation nano electronic devices, showing great potential to extend the scaling limits in silicon-based complementary metal oxide semiconductor (CMOS) field-effect transistors (FETs).

As one of the most studied TMD materials, tungsten diselenide ( $\text{WSe}_2$ ) possesses three dominant polymorphs, including the semiconducting trigonal prismatic (2H phase), metallic octahedral (1T phase), and distorted octahedral (1T' phase). 2H semiconducting  $\text{WSe}_2$  demonstrates great advantages in complementary logic devices, arising from its ambipolar transport property with high current on/off ratio. However, similar to other TMDs, 2H  $\text{WSe}_2$ -based transistors generally suffer from high Schottky barrier height and high contact resistance at the metal contact/ $\text{WSe}_2$  interface, which degrades the performance of  $\text{WSe}_2$  FETs, including the electrical conductance and carrier mobility.

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To reduce contact resistance in  $\text{WSe}_2$ -based FETs, various methods are currently being explored, such as metal contact engineering, ionic liquid gating, photo-doping, and surface charge transfer doping.

15 Several approaches have also been employed to induce 2H to 1T/1T' phase transition in TMDs, such as alkali metal intercalation, strain engineering, ionic liquid gating and laser irradiation. However, alkali metal intercalation requires soaking the TMD in a chemical liquid such as n-butyllithium (n-BuLi) or tert-butyl lithium (t-BuLi) which is both complicated and time-consuming. Strain engineering and ionic liquid gating  
20 require harsh conditions to be successful. High energy laser irradiation results in undesirable and irreversible damage to samples.

There is a continuing need to improve the performance of electronic devices based on TMD materials.

## 5 Summary

In a first aspect, a material is provided, the material comprising: a transition metal dichalcogenide (TMD) comprising a surface, a least a portion of the surface being surface-modified with one or more Group 1 metals, wherein the one or more Group 1 metals comprise Cs and/or Rb.

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A transition metal dichalcogenide (TMD) has the general formula  $MX_2$ , where M is a transition metal atom and X is a chalcogen atom.

The transition metal dichalcogenide may comprise one or more of  $MoS_2$ ,  $WS_2$ ,  $MoSe_2$  and  $WSe_2$ ,  $MoTe_2$ , alkali metal-doped  $MoTe_2$ , alkali metal-doped  $MoSe_2$ , alkali metal-doped  $MoS_2$ , alkali metal-doped  $WSe_2$ , and alkali metal-doped  $WS_2$ . The transition metal dichalcogenide may comprise one or more of  $WSe_2$  and/or  $MoTe_2$ . The transition metal dichalcogenide may comprise  $WSe_2$ .

20 The TMD may comprise one or more impurities.

The transition metal dichalcogenide may be substantially two-dimensional (2-D). A portion of the transition metal dichalcogenide may be substantially two-dimensional. A portion or all of the transition metal dichalcogenide may have a thickness of between 1  
5 and 5 layers. A portion or all of the transition metal dichalcogenide may comprise a mono-layer or a bi-layer.

'Surface modified' or 'surface modification' refers to a surface of a material being changed by bringing physical, chemical or biological characteristics different from the  
10 ones originally found on the surface of a material. For example, a surface is modified if it is functionalised by adding new functions, features, capabilities, or properties to a material. The modification changes the surface chemistry of the material. In this regard, the modification or functionalisation resides only on the surface and does not penetrate the material. In contrast, 'doping' refers to the intentional introduction of  
15 impurities into an intrinsic semiconductor for the purpose of modulating its electrical, optical and structural properties. In this regard, the impurity resides within the semiconductor.

One portion of the surface of the TMD may be surface-modified and one portion may  
20 not be surface modified. All of the surface may be surface modified. A plurality of

portions of the surface may be surface-modified. The surface may be modified by a mixture of two or more alkali metals. The surface may be modified only by Caesium and/or Rubidium. One portion of the TMD may be surface modified with Caesium and/or Rubidium and another portion may be surface modified with another alkali metal. The one or more alkali metals may comprise one or more impurities.

The one or more alkali metals may comprise Caesium and one or more element selected from Lithium, Sodium, Potassium and Rubidium.

The one or more alkali metals may comprise Rubidium and one or more element selected from Lithium, Sodium, Potassium and Caesium.

The alkali metal may be in direct contact with the surface of the TMD. There may be a direct interface between the alkali metal and the TMD.

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The one or more Group 1 metals may form a layer on the surface of the TMD. The layer of Group 1 metal may have a thickness of greater than or equal to 0.2nm. The layer may have a thickness of less than or equal to 5.0nm. The layer of Group 1 metal may have a thickness of between 0.4nm and 2.0nm.

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For the avoidance of doubt, it is explicitly contemplated that where a number of numerical ranges related to the same feature are cited herein, that the end points for each range are intended to be combined in any order to provide further contemplated (and implicitly disclosed) ranges. Thus, in relation to the above related numerical

5 ranges, there is disclosed:

0.0nm to 0.01nm, 0.0nm to 0.05nm, 0.0nm to 0.07nm, 0.0nm to 0.08nm, 0.0nm to 0.1nm, 0.0nm to 0.19nm, 0.0nm to 0.20nm, 0.0nm to 0.4nm 0.0nm to 0.5nm, 0.0nm to 0.6nm 0.0nm to 1.0nm, 0.0nm to 2.0nm, 0.0nm to 5.0nm;

0.01nm to 0.05nm, 0.01nm to 0.07nm, 0.01nm to 0.08nm, 0.01nm to 0.1nm, 0.01nm  
10 to 0.19nm, 0.01nm to 0.20nm, 0.01nm to 0.4nm 0.01nm to 0.5nm, 0.01nm to 0.6nm  
0.01nm to 1.0nm, 0.01nm to 2.0nm, 0.01nm to 5.0nm;

0.05nm to 0.07nm, 0.05nm to 0.08nm, 0.05nm to 0.1nm, 0.05nm to 0.19nm, 0.05nm  
to 0.20nm, 0.05nm to 0.4nm 0.05nm to 0.5nm, 0.05nm to 0.6nm 0.05nm to 1.0nm,  
0.05nm to 2.0nm, 0.05nm to 5.0nm;

0.07nm to 0.08nm, 0.07nm to 0.1nm, 0.07nm to 0.19nm, 0.07nm to 0.20nm, 0.07nm  
15 to 0.4nm 0.07nm to 0.5nm, 0.07nm to 0.6nm 0.07nm to 1.0nm, 0.07nm to 2.0nm,  
0.07nm to 5.0nm;

0.08nm to 0.1nm, 0.08nm to 0.19nm, 0.08nm to 0.20nm, 0.08nm to 0.4nm 0.08nm to  
0.5nm, 0.08nm to 0.6nm 0.08nm to 1.0nm, 0.08nm to 2.0nm, 0.08nm to 5.0nm;

0.10nm to 0.19nm, 0.10nm to 0.20nm, 0.10nm to 0.4nm, 0.10nm to 0.5nm, 0.10nm to  
20 0.6nm 0.10nm to 1.0nm, 0.10nm to 2.0nm, 0.10nm to 5.0nm;

0.19nm to 0.20nm, 0.19nm to 0.4nm, 0.19nm to 0.5nm, 0.19nm to 0.6nm 0.19nm to 1.0nm, 0.19nm to 2.0nm, 0.19nm to 5.0nm;

0.2nm to 0.4nm, 0.2nm to 0.5nm, 0.2nm to 0.6nm 0.2nm to 1.0nm, 0.2nm to 2.0nm, 0.2nm to 5.0nm;

5 0.4nm to 0.5nm, 0.4nm to 0.6nm, 0.4nm to 1.0nm, 0.4nm to 2.0nm, 0.4nm to 5.0nm;

0.5nm to 0.6nm, 0.5nm to 1.0nm, 0.5nm to 2.0nm, 0.5nm to 5.0nm;

0.6nm to 1.0nm, 0.6nm to 2.0nm, 0.6nm to 5.0nm;

1.0nm to 2.0nm, 1.0nm to 5.0nm; and

2.0nm to 5.0nm.

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The surface modified portion or portions of the TMD may be in a different phase to the portion or portions of the TMD that are not surface modified. The surface-modified portion or portions may be in a 1T or 1T' phase and the portion or portions that are not surface-modified may be in a 2H phase.

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As is known in the art, '2H' refers to the hexagonal phase structure and '1T' refers to the metallic monoclinic or octahedral phase structure.

In an aspect, an electronic device comprising a transition metal dichalcogenide (TMD) is provided, the TMD comprising first and second portions which are surface modified with one or more a Group 1 metals and a third portion which is not surface modified with one or more Group 1 metals; and first and second electrodes, wherein the first and second electrodes are in direct electrical contact with the first and second portions of the transition metal dichalcogenide, respectively, wherein the one or more Group 1 metals comprises Caesium and/or Rubidium.

The transition metal dichalcogenide may comprise one or more of  $\text{MoS}_2$ ,  $\text{WS}_2$ ,  $\text{MoSe}_2$  and  $\text{WSe}_2$ ,  $\text{MoTe}_2$ , alkali metal-doped  $\text{MoTe}_2$ , alkali metal-doped  $\text{MoSe}_2$ , alkali metal-doped  $\text{MoS}_2$ , alkali metal-doped  $\text{WSe}_2$ , and alkali metal-doped  $\text{WS}_2$ . The transition metal dichalcogenide may comprise one or more of  $\text{WSe}_2$  and/or  $\text{MoTe}_2$ . The transition metal dichalcogenide may comprise  $\text{WSe}_2$ .

The one or more alkali metals may comprise Caesium and the transition metal dichalcogenide may comprise  $\text{WSe}_2$ .

The TMD may comprise one or more impurities.

The transition metal dichalcogenide may be substantially two-dimensional (2-D). A portion of the transition metal dichalcogenide may be substantially two-dimensional. A portion or all of the transition metal dichalcogenide may have a thickness of between 1 and 5 layers. A portion or all of the transition metal dichalcogenide may comprise a  
5 mono-layer or a bi-layer.

The surface may be modified by a mixture of two or more alkali metals. The surface may be modified only by Caesium and/or Rubidium. One portion of the TMD may be surface modified with Caesium and/or Rubidium and another portion may be surface  
10 modified with another alkali metal. The one or more alkali metals may comprise one or more impurities.

The one or more Group 1 metals may form a layer on the surface of the TMD. The layer of Group 1 metal may have a thickness of greater than or equal to 0.2nm. The  
15 layer may have a thickness of less than or equal to 5.0nm. The layer of Group 1 metal may have a thickness of between 0.4nm and 2.0nm.

The thickness of the more or more alkali metals may fall into one of the following ranges: 0.0nm to 0.01nm, 0.0nm to 0.05nm, 0.0nm to 0.07nm, 0.0nm to 0.08nm,  
20 0.0nm to 0.1nm, 0.0nm to 0.19nm, 0.0nm to 0.20nm, 0.0nm to 0.4nm 0.0nm to 0.5nm, 0.0nm to 0.6nm 0.0nm to 1.0nm, 0.0nm to 2.0nm, 0.0nm to 5.0nm; 0.01nm to

0.05nm, 0.01nm to 0.07nm, 0.01nm to 0.08nm, 0.01nm to 0.1nm, 0.01nm to 0.19nm,  
 0.01nm to 0.20nm, 0.01nm to 0.4nm 0.01nm to 0.5nm, 0.01nm to 0.6nm 0.01nm to  
 1.0nm, 0.01nm to 2.0nm, 0.01nm to 5.0nm; 0.05nm to 0.07nm, 0.05nm to 0.08nm,  
 0.05nm to 0.1nm, 0.05nm to 0.19nm, 0.05nm to 0.20nm, 0.05nm to 0.4nm 0.05nm to  
 5 0.5nm, 0.05nm to 0.6nm 0.05nm to 1.0nm, 0.05nm to 2.0nm, 0.05nm to 5.0nm;  
  
 0.07nm to 0.08nm, 0.07nm to 0.1nm, 0.07nm to 0.19nm, 0.07nm to 0.20nm, 0.07nm  
 to 0.4nm 0.07nm to 0.5nm, 0.07nm to 0.6nm 0.07nm to 1.0nm, 0.07nm to 2.0nm,  
 0.07nm to 5.0nm; 0.08nm to 0.1nm, 0.08nm to 0.19nm, 0.08nm to 0.20nm, 0.08nm to  
 0.4nm 0.08nm to 0.5nm, 0.08nm to 0.6nm 0.08nm to 1.0nm, 0.08nm to 2.0nm,  
 10 0.08nm to 5.0nm; 0.10nm to 0.19nm, 0.10nm to 0.20nm, 0.10nm to 0.4nm, 0.10nm to  
 0.5nm, 0.10nm to 0.6nm 0.10nm to 1.0nm, 0.10nm to 2.0nm, 0.10nm to 5.0nm;  
  
 0.19nm to 0.20nm, 0.19nm to 0.4nm, 0.19nm to 0.5nm, 0.19nm to 0.6nm 0.19nm to  
 1.0nm, 0.19nm to 2.0nm, 0.19nm to 5.0nm; 0.2nm to 0.4nm, 0.2nm to 0.5nm, 0.2nm  
 to 0.6nm 0.2nm to 1.0nm, 0.2nm to 2.0nm, 0.2nm to 5.0nm; 0.4nm to 0.5nm, 0.4nm  
 15 to 0.6nm, 0.4nm to 1.0nm, 0.4nm to 2.0nm, 0.4nm to 5.0nm; 0.5nm to 0.6nm, 0.5nm  
 to 1.0nm, 0.5nm to 2.0nm, 0.5nm to 5.0nm; 0.6nm to 1.0nm, 0.6nm to 2.0nm, 0.6nm  
 to 5.0nm; 1.0nm to 2.0nm, 1.0nm to 5.0nm; and 2.0nm to 5.0nm.

The surface modified portion or portions of the TMD may be in a different phase to the  
 20 portion or portions of the TMD that are not surface modified. The surface-modified

portion or portions may be in a 1T or 1T' phase and the portion or portions that are not surface-modified may be in a 2H phase.

The device may exhibit substantially Ohmic contact behaviour with respect to the first  
5 and second electrodes. In this context, Ohmic contact behaviour implies that the current between the two electrodes of the device has a substantially linear dependence on voltage.

The device may have a Schottky barrier height of less than or equal to 10meV. The  
10 device may have a Schottky barrier height of less than or equal to 9.4meV. The device may have a Schottky barrier height of between 9meV and 10meV or of between 9.4meV and 10meV.

The device may have a field effect electron mobility at room temperature (298K) of  
15  $35 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  or greater, particularly  $37.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  or greater, more particularly  $70 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  or greater. The device may have a field effect electron mobility at room temperature (298K) falling in one of the following ranges:  $35 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  to  $37.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ,  $35 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  to  $70 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ,  $35 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  to  $75 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ;  $37.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  to  $70 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ,  $37.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  to  $75 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ;  $70 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  to  $75 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ .

The device may have a current on/off ratio at room temperature (298K) of  $10^6$  or greater, particularly  $10^7$  or greater, further particularly  $10^8$  or greater. The device may have a current on/off ratio of approximately  $10^9$ . The device may have a current on/off ratio at room temperature falling in one of the following ranges:  $10^6$  to  $10^7$ ,  $10^6$  to  $10^8$ ,  
5  $10^6$  to  $10^9$ ;  $10^7$  to  $10^8$ ,  $10^7$  to  $10^9$ ; and  $10^8$  to  $10^9$ .

The device may have a subthreshold swing at room temperature (298K) of  $85\text{mV dec}^{-1}$  or less, particularly  $75\text{mV dec}^{-1}$  or less, further particularly in the range  $60\text{ mV dec}^{-1}$  to  $75\text{ mV dec}^{-1}$ . The device may have a subthreshold swing of  $61\text{ mV dec}^{-1}$ . The device  
10 may have a subthreshold swing falling in one of the following ranges:  $60\text{ mV dec}^{-1}$  to  $61\text{ mV dec}^{-1}$ ,  $60\text{ mV dec}^{-1}$  to  $75\text{ mV dec}^{-1}$ ,  $60\text{ mV dec}^{-1}$  to  $85\text{ mV dec}^{-1}$ ;  $61\text{ mV dec}^{-1}$  to  $75\text{ mV dec}^{-1}$ ,  $61\text{ mV dec}^{-1}$  to  $85\text{ mV dec}^{-1}$ ; and  $75\text{mV dec}^{-1}$  to  $85\text{ mV dec}^{-1}$ .

The electronic device may be a field-effect transistor.

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The electronic device may be a logic inverter. The inverter may be capable of a gain greater than 100. The inverter may be capable of a gain of greater than 5 with a power consumption less than 10 pW.

The material and/or device may be held under substantially vacuum conditions. The device may be operated under substantially vacuum conditions. The device may further comprise a vacuum chamber configured to contain the surface-modified TMD under substantially vacuum conditions. By substantially vacuum conditions, it is  
5 intended to mean pressures of  $10^{-7}$  mbar or less.

The material and/or device may be held under a nitrogen atmosphere. The material and/or device may be packaged with a nitrogen atmosphere. The nitrogen atmosphere may be a substantially 100% nitrogen environment.

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The material and/or device may comprise a package configured or arranged to exclude oxygen and water from contact with the surface-modified TMD. The package may be configured to maintain the surface-modified TMD under vacuum. The package may be configured to maintain the surface-modified TMD in a Nitrogen ( $N_2$ ) or other inert  
15 atmosphere.

In an aspect, a method of producing a material is provided, the material comprising: a transition metal dichalcogenide (TMD) comprising a surface, a least a portion of the surface being surface-modified with one or more Group 1 metals, wherein the one or  
20 more Group 1 metals comprise Cs and/or Rb, the method comprising: providing a transition metal dichalcogenide; and evaporating one or more Group 1 metals onto at

least a portion of a surface of the transition metal dichalcogenide, wherein the one or more group 1 metals comprises Cs and/or Rb.

In an aspect, a method of producing an electronic device is provided, the electronic  
5 device comprising: a transition metal dichalcogenide (TMD), the TMD comprising first  
and second portions which are surface modified with one or more a Group 1 metals  
and a third portion which is not surface modified with one or more Group 1 metals;  
and first and second electrodes, wherein the first and second electrodes are in direct  
electrical contact with the first and second portions of the transition metal  
10 dichalcogenide, respectively, wherein the one or more Group 1 metals comprises  
Caesium and/or Rubidium, the method comprising: providing a layer of transition  
metal dichalcogenide and first and second electrodes on the surface of a substrate,  
such that the first and second electrodes are in electrical contact with the layer of  
transition metal dichalcogenide; evaporating one or more Group 1 metals onto a  
15 surface of first and second portions of the layer of transition metal dichalcogenide  
such that the one or more Group 1 metals has a thickness of at least 0.2nm, wherein  
the first and second portions of the layer of transition metal dichalcogenide are  
adjacent to the first and second electrodes respectively, and wherein the one or more  
Group 1 metals comprises Cs and/or Rb.

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#### Brief description of Figures

Embodiments are described below in association with the Figures, in which:

Figure 1 shows a material according to an embodiment;

Figure 2 shows a material according to an embodiment;

Figures 3a and 3b show the 2H and 1T' phases of WSe<sub>2</sub>, respectively;

5 Figure 4 shows a device according to an embodiment;

Figure 5 shows a device according to an embodiment;

Figure 6 shows a device according to an embodiment;

Figure 7 shows a method of producing a material according to an embodiment;

Figure 8a shows the line profile derived from the Atomic Force Microscope (AFM)

10 image of a bilayer WSe<sub>2</sub> device;

Figure 8b shows Raman measurements for the bilayer WSe<sub>2</sub> device;

Figure 8c shows photoluminescence (PL) measurements for the bilayer WSe<sub>2</sub> device;

Figure 9a shows a schematic representation of a bilayer WSe<sub>2</sub> device with surface modification;

15 Figure 9b and Figure 9c show transport characteristics ( $I_{sd}$ - $V_g$ ) of a pristine bilayer WSe<sub>2</sub> FET;

Figure 9d shows transfer characteristic evolution of the WSe<sub>2</sub> FET as a function of Cs thickness;

Figure 9e shows the electrical conductance (G) versus Cs thickness at  $V_g = 0V$  of the

20 WSe<sub>2</sub> FET;

Figure 9f shows output curves ( $I_{sd}$ - $V_{sd}$ ) for the pristine and 1.0 nm Cs-modified WSe<sub>2</sub> FET;

Figures 9g and 9h show temperature-dependent transport measurements for the Cs-modified WSe<sub>2</sub> FET;

Figure 9i shows the electrical conductance evolution of the bilayer WSe<sub>2</sub> device after 1.0 nm Cs functionalization with respect to temperature at different V<sub>g</sub>;

5 Figure 10 (a)-(d) show the results of in situ XPS and UPS of the bilayer WSe<sub>2</sub> device;

Figure 11a shows the Photoluminescence (PL) spectra for a bilayer WSe<sub>2</sub> flake before and after 0.1 nm Cs modification;

Figure 11b shows Raman measurements for a bilayer WSe<sub>2</sub> flake before and after 0.1 nm Cs modification;

10 Figure 12a shows the evolution of transfer characteristics of a device according to an embodiment as a function of Cs thickness;

Figure 12b shows the evolution of field-effect electron mobility for the device;

Figures 12c and Figure 12d illustrate the output curves of the device under a range of gate voltages after and before Cs modification, respectively;

15 Figure 13a shows the Schottky barrier height of a hetero-phase transistor according to an embodiment;

Figure 13b shows the width-normalized total resistance ( $R_{\text{tot}}$ ) as a function of the channel length at V<sub>g</sub> = 5 V for the hetero-phase transistor;

Figure 14a shows the transfer characteristic evolution of the device as a function of Cs

20 thickness for a sandwich framework device according to an embodiment;

Figure 14b shows the corresponding electron mobility versus Cs thickness;

Figures 14c and 14d show output curves for the device before and after 1.0 nm Cs contact doping at different gate voltages ranging from 1 V to 5 V, respectively;

Figure 14e shows the transfer characteristic evolution of the device as a function of Cs thickness for another sandwich framework device according to an embodiment;

5 Figure 15a shows transfer characteristics for a logic inverter according to an embodiment;

Figure 15b shows output characteristics of the inverter;

Figure 15c shows the extracted gain as a function of  $V_{IN}$  at three different  $V_{DD}$  for the inverter;

10 Figure 15d shows the evolution of the power consumption of the inverter versus  $V_{DD}$ ;

Figure 16 (a) shows output characteristics of a homogeneous WSe<sub>2</sub> inverter according to an embodiment; and

Figure 16 (b) shows the output curve and corresponding voltage gain as a function of  $V_{IN}$  for the inverter.

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### Detailed Description

For purposes of brevity and clarity, descriptions of embodiments of the present disclosure are directed to a transition metal dichalcogenide and uses thereof, in accordance with the drawings. While aspects of the present disclosure will be

20 described in conjunction with the embodiments provided herein, it will be understood that they are not intended to limit the present disclosure to these embodiments. On the contrary, the present disclosure is intended to cover alternatives, modifications

and equivalents to the embodiments described herein, which are included within the scope of the present disclosure as defined by the appended claims. Furthermore, in the following detailed description, specific details are set forth in order to provide a thorough understanding of the present disclosure. However, it will be recognized by an individual having ordinary skill in the art, i.e. a skilled person, that the present disclosure may be practiced without specific details, and/or with multiple details arising from combinations of aspects of particular embodiments. In a number of instances, well-known systems, methods, procedures, and components have not been described in detail so as to not unnecessarily obscure aspects of the embodiments of the present disclosure.

In embodiments of the present disclosure, depiction of a given element or consideration or use of a particular element number in a particular figure or a reference thereto in corresponding descriptive material can encompass the same, an equivalent, or an analogous element or element number identified in another figure or descriptive material associated therewith.

References to “an embodiment / example”, “another embodiment / example”, “some embodiments / examples”, “some other embodiments / examples”, and so on, indicate that the embodiment(s) / example(s) so described may include a particular feature, structure, characteristic, property, element, or limitation, but that not every

embodiment / example necessarily includes that particular feature, structure, characteristic, property, element or limitation. Furthermore, repeated use of the phrase “in an embodiment / example” or “in another embodiment / example” does not necessarily refer to the same embodiment / example.

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The terms “comprising”, “including”, “having”, and the like do not exclude the presence of other features / elements / steps than those listed in an embodiment, nor do they require the presence of other features. Recitation of certain features / elements / steps in mutually different embodiments does not indicate that a  
10 combination of these features / elements / steps cannot be used in an embodiment.

As used herein, the terms “a” and “an” are defined as one or more than one. The use of “/” in a figure or associated text is understood to mean “and/or” unless otherwise indicated. The recitation of a particular numerical value or value range herein is  
15 understood to include or be a recitation of an approximate numerical value or value range.

Figure 1 shows a schematic representation of a material 1 according to an embodiment. In the embodiment of Figure 1, the material comprises a layer 101 of a  
20 transmission metal dichalcogenide (TMD).

On the surface 109 of the TMD 101, is provided a layer 103 of one or more alkali metals, i.e. the surface of the TMD is surface-modified with one or more alkali metals. In the embodiment of Figure 1, alkali metal is provided on the surface of two portions 105 of the TMD 101. In the embodiment of Figure 1, a portion 107 of the TMD, 5 positioned between the regions 105 is not surface modified by alkali metal 103. In other embodiments, all of the TMD may be surface modified or only one or a greater number of portions of the TMD may be surface modified.

The thickness of the TMD is not particularly limited. In embodiments, the TMD may be 10 provided as a monolayer, a bilayer or as a multilayer, for example with a thickness of 3-5 layers. However, monolayer, bilayer or otherwise substantially two-dimensional forms of TMD may be advantageous for use in electronic devices, enabling low-profile devices to be provided.

15 The thickness of a TMD layer may be approximately determined by using a high-resolution optical microscope (e.g. the Nikon Eclipse LV100D), and further confirmed by Atomic Force Microscopy (AFM).

In an embodiment, the layer of alkali metal comprises Caesium and/or Rubidium.

In an embodiment, the layer of alkali metal comprises a mixture of more than one alkali metal.

The layer of alkali metal may comprise Caesium and one or more element selected  
5 from Lithium, Sodium, Potassium and Rubidium.

The layer of alkali metal may comprise Rubidium and one or more element selected from Lithium, Sodium, Potassium and Caesium.

10 In an embodiment, the thickness of the alkali metal layer is in the range 0.2nm to 5nm.  
In an embodiment, the thickness of the alkali metal may be in the range 0.4nm to 2nm.  
In an embodiment, the thickness of Caesium and/or Rubidium is in the range 0.2nm to 5nm. In an embodiment, the thickness of Caesium and/or Rubidium may be in the range 0.4nm to 2nm. Thicknesses lying in this range may convey advantageous  
15 electronic properties to the surface-modified portions 105 of the TMD. These properties will be discussed further below.

The thickness of the alkali metal layer may be determined by weight, for example, using a quartz crystal microbalance.

X-ray photoelectron spectroscopy (XPS) can also be employed to determine the thickness of the alkali metal. One such protocol suitable for determining the thickness of the alkali metal is given in the reference: Seah, M. P., & Dench, W. A. (1979), Quantitative electron spectroscopy of surfaces: A standard data base for electron inelastic mean free paths in solids. *Surf. Interface Anal.*, 1(1), 2-11.

In an embodiment, the TMD may be selected from MoS<sub>2</sub>, WS<sub>2</sub>, MoSe<sub>2</sub> and WSe<sub>2</sub>, MoTe<sub>2</sub>, alkali metal-doped MoTe<sub>2</sub>, alkali metal-doped MoSe<sub>2</sub>, alkali metal-doped MoS<sub>2</sub>, alkali metal-doped WSe<sub>2</sub>, and alkali metal-doped WS<sub>2</sub>.

10

In particular, the TMD may be selected from WSe<sub>2</sub> and MoTe<sub>2</sub>. More particularly, the TMD may be WSe<sub>2</sub>.

In an embodiment, the alkali metal may comprise Caesium and/or Rubidium and the TMD may be selected from MoS<sub>2</sub>, WS<sub>2</sub>, MoSe<sub>2</sub> and WSe<sub>2</sub>, MoTe<sub>2</sub>, alkali metal-doped MoTe<sub>2</sub>, alkali metal-doped MoSe<sub>2</sub>, alkali metal-doped MoS<sub>2</sub>, alkali metal-doped WSe<sub>2</sub>, and alkali metal-doped WS<sub>2</sub>. In particular, the alkali metal may comprise Caesium and/or Rubidium and the TMD may be selected from WSe<sub>2</sub> and MoTe<sub>2</sub>. More particularly, alkali metal may comprise Caesium and/or Rubidium and the TMD may comprise tungsten diselenide (WSe<sub>2</sub>).

20

A material according to this embodiment is shown in Figure 2, which is a schematic representation of WSe<sub>2</sub> surface modified with Cs. In the embodiment of Figure 2, WSe<sub>2</sub> is provided as a monolayer. However, in other embodiments, WSe<sub>2</sub> may be provided as a bilayer or as a multilayer (for example, between 3 and 5 layers) material.

5

In an embodiment, the portion 107 of TMD 101 which is not surface modified (if present) may have a 2H crystal structure. In an embodiment the surface modification of the portion or portions 105 of TMD 101 may result in these portions having a different phase from the portion 107 which is not surface modified. In an embodiment, the portion or portions 105 may have a 1T or 1T' crystal structure, particularly a 1T' crystal structure. Figures 3a and 3b show the 2H and 1T' crystal structures of WSe<sub>2</sub>, respectively, with Tungsten atoms denoted by 301 and the Selenium atoms denoted by 303.

15 High-resolution transmission electron microscope (HRTEM) can be employed to directly observe the atomically sharp interface between the 2H and 1T/1T' phases in materials according to embodiments. A protocol suitable for such characterisation is given in, for example, Koppera, R., et al. *Nat. Mater.* 13.12 (2014): 1128.

20 The crystal structure of the TMD in the surface modified portions may depend on the thickness of the alkali metal layer 103 present on the surface. In embodiments, the

thickness of the alkali metal 103 may be chosen such that the surface-modified portions 105 of the TMD have a substantially 1T or 1T' crystal structure. Typically, the TMD will exhibit 1T or 1T' behaviour at larger thicknesses of alkali metal, as shown in the experimental results discussed below.

5

In an embodiment, the portion 107 of TMD 101 that is not surface modified may be a semi-conductor. In embodiments, the surface modification of the portion or portions 105 may result in these portions exhibiting different electrical behaviour than the portion 107 of TMD that is not surface modified. In an embodiment, the portion, or  
10 portions 105 may exhibit metallic behaviour. In an embodiment, the portion, or portions 105 may exhibit n-type doping behaviour.

The electrical behaviour of the surface-modified and unmodified portions can be determined by examining the electrical transport properties of the material in  
15 accordance with methods well known in the art.

In an embodiment, the electrical behaviour of surface modified portions of the TMD may depend on the thickness of the layer of alkali metal 103 on their respective surfaces. In an embodiment, the thickness of the layer of alkali metal may be selected  
20 such that the surface modified portions of the TMD 105 exhibit metallic or

substantially metallic behaviour. Typically, the surface-modified portions of TMD will exhibit metallic behaviour at larger thicknesses of alkali metal.

In other embodiments, the thickness of the alkali metal may be selected in order to  
5 obtain other electrical behaviours, such as n-type doping behaviour relative to the non-surface modified TMD.

In an embodiment, the thickness of the alkali metal is in the range 0.2nm to 5nm. In an  
embodiment, the thickness of the alkali metal may be in the range 0.4nm to 2nm. In  
10 this embodiment, the TMD may exhibit metallic behaviour and Ohmic contact behaviour.

In an embodiment, the thickness of the alkali metal layer may be less than 0.4nm. In an  
embodiment, the thickness of the alkali metal layer may be between 0.2nm and  
15 0.4nm. In this embodiment, the TMD may exhibit n-type doping behaviour of the surface-modified portions 105 of the TMD relative to the non-surface modified portions 107.

In an embodiment, the thickness of Caesium and/or Rubidium is in the range 0.2nm to  
20 5nm. In an embodiment, the thickness of Caesium and/or Rubidium may be in the

range 0.4nm to 2nm. In this embodiment, the TMD may exhibit metallic behaviour and Ohmic contact behaviour.

In an embodiment, the thickness of Caesium and/or Rubidium may be less than 0.4nm.

5 In an embodiment, the thickness of Caesium and/or Rubidium may be between 0.2nm and 0.4nm. In this embodiment, the TMD may exhibit n-type doping behaviour of the surface-modified portions 105 of the TMD relative to the non-surface modified portions 107.

10 According to embodiment described above the material of Figure 1 may comprise a hetero-phase contact within the TMD layer at the interface 111 between the surface-modified and unmodified portions. In embodiments, the hetero-phase contact is between a 2H phase in the portions which are not surface modified and a 1T' phase in the portions which are surface modified.

15

Thus, materials according to these embodiments above may enable the exploitation of the both the semiconducting and metallic properties of two phases of TMD within the same material, namely both the advantageous ambipolar transport properties of the 2H phase and the advantageous ohmic electrical contact via surface-doped metallic 1T'

20 portions.

In particular, materials according to embodiments described above may be advantageously deployed in electronic devices such as transistors by employing the metallic 1T/1T' phased TMD as a buffer contact layer, thereby achieving 2H-1T/1T' hetero-phase transistors with low contact resistance and Ohmic behaviour.

5

In contrast to the metal contacts in existing 2D TMD transistors, 2H-1T/1T' heterophase contact in materials according to embodiments described above can i) avoid the lattice mismatch between the metal electrodes and the channel materials, which significantly enhances the carrier injection efficiency; ii) eliminate the Fermi  
10 level pinning effect originating from the surface states; iii) and create an atomically sharp interface, to avoid the chemical bond formation at the metal/semiconductor interface which can generate large strain in the crystal lattice.

As shown below in the Examples, surface-modification with Caesium and/or Rubidium  
15 results in devices with highly advantageous electrical properties.

Surface modification using alkali metals, particularly Caesium and/or Rubidium, in order to obtain heterophase contact in TMDs as described above provides a facile, non-destructive method to achieve Ohmic contact for 2D materials, while maintaining  
20 ambipolar behaviour. Indeed, the alkali metal surface functionalization, particularly surface functionalization using Caesium and/or Rubidium, can be performed in situ as

will be discussed further below. Phase transition performed in this way also enables a high degree of control over the area of TMD which undergoes the phase transition.

With conventional semiconductors, ion implantation and thermal diffusion have been  
5 extensively employed to accurately modulate different carrier concentrations within them. However, in 2D materials, these doping techniques may destroy the crystal lattice or induce substantial defects into the materials due to their atomically thin nature, thus deteriorating their intrinsic properties. In contrast, surface modification is particularly effective in 2-D materials due to their large surface-body ratio.

10

### Devices

In an embodiment, the material according to the above described embodiments is employed in electronic device. In an embodiment, the material according to Figure 1 is  
15 employed in a Field effect transistor (FET).

A schematic of a n-type FET device according to this embodiment is shown in Figure 4.

In this embodiment, the transistor comprises a monolayer of TMD 101 arranged on a  
20 substrate 401. In the embodiment of Figure 4 the substrate is a p-type Silicon wafer

with SiO<sub>2</sub> layer. The skilled person will appreciate that other suitable substrates with insulating properties may be employed according to embodiments.

Source and drain electrodes 403 are provided on the substrate at either end of the TMD layer 101. The reason for this arrangement will become apparent from the discussion below. In the embodiment of Figure 4, the electrodes 403 comprise Palladium (Pd). However, the person skilled in the art will appreciate that other suitable metallic materials may be employed according to embodiments.

In this embodiment, a layer of photoresist material 405 is arranged on a portion the surface of the TMD layer 101. In the embodiment of Figure 4, a photoresist such as PMMA is employed due to its photoresist properties which are advantageously employed during the manufacturing process (see below). In other embodiment, the top layer of 405 may be any insulating material capable of encapsulating the TMD layer 101 to avoid modification with one or more alkali metals including Cs and/or Rb modification. In embodiments, the photoresist or other insulating layer 405 may be omitted partially or completely.

In an embodiment, the ends 105 of the TMD layer adjacent to the source and drain electrodes 403 are not covered by the dielectric 405, i.e. they are exposed.

In an embodiment, a back-gate electrode (not shown) is arranged on the Silicon substrate.

An alkali metal layer 103 is present on the portion of the surface at either end of the  
5 TMD layer 101 which is not covered by the photoresist 405. The TMD layer 101 is therefore surface modified at each end 105 but is unmodified in the centre. In an embodiment, the alkali metal layer comprises Caesium and/or Rubidium.

In an embodiment, the TMD may be selected from  $\text{MoS}_2$ ,  $\text{WS}_2$ ,  $\text{MoSe}_2$  and  $\text{WSe}_2$ ,  
10  $\text{MoTe}_2$ , alkali metal-doped  $\text{MoTe}_2$ , alkali metal-doped  $\text{MoSe}_2$ , alkali metal-doped  $\text{MoS}_2$ , alkali metal-doped  $\text{WSe}_2$ , and alkali metal-doped  $\text{WS}_2$ .

In particular, the TMD may be selected from  $\text{WSe}_2$  and  $\text{MoTe}_2$ . More particularly, the TMD may be  $\text{WSe}_2$ .

15

In an embodiment, the width of each of the portions of the TMD layer on which alkali metal is present is in the range 0.2-5  $\mu\text{m}$ . In an embodiment, they have a width in the range 0.2-0.3  $\mu\text{m}$ .

As explained above, beyond a certain thickness of alkali metal, the TMD layer may be metallic at each end 105 but behave as a semiconductor towards the centre of the layer 107, in the region 107 positioned under the photoresist 405. In the embodiment of Figure 4, the TMD is employed as a n-type unipolar semiconductor. In an  
5 embodiment, the TMD has a 1T or 1T' phase at each end 105 adjacent to the source and drain electrodes 403 and a 2H phase in the portion 107 beneath the gate electrode which is not surface modified with alkali metal. The TMD is therefore comprises a hetero-phase contact 111 and the device 4 is therefore a hetero-phase transistor.

10 In an embodiment, the thickness of the alkali metal lies in the range 0.2nm to 5nm. In an embodiment, it lies in the range 0.4nm-2nm as this ensures good ohmic contact between the source and drain electrodes and the TMD, as will be shown in the Examples discussed below. In an embodiment, the thickness of the alkali metal is approximately 1.0nm.

15

In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the thickness of the Caesium and/or Rubidium lies in the range 0.2nm to 5nm. In an embodiment, it lies in the range 0.4nm-2nm. In an embodiment, the thickness of the Caesium and/or Rubidium is approximately 1.0nm.

20

In an embodiment, the thickness of the alkali metal is chosen according to the desired properties of the device.

In an embodiment, the thickness of the alkali metal is chosen such that there is  
5 substantially ohmic contact between the electrodes and the TMD layer, i.e. the current between the source and drain electrodes 403 has a substantially linear dependence on voltage.

In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the  
10 thickness of the alkali metal is such that the current on/off ratio of the device 4 at room temperature (298K) is at least  $10^6$ .

The current on/off ratio of the device is defined by the ratio of the on state current and off state current, i.e. it is the ratio of the current maximum and the current  
15 minimum in the transfer characteristic curve.

In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the thickness of the alkali metal is such that the field-effect electron mobility in the device at room temperature (298K) is at least  $30 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ .

The field effect electron mobility  $\mu$  of the device is derived from the linear regime of a transfer plot of current between source and drain electrodes ( $I_{sd}$ ) against potential difference across the source and drain electrodes ( $V_{sd}$ ) using the equation:

$$\mu = \frac{L}{WC_i V_{sd}} \frac{dI_{sd}}{dV_{sd}}$$

5 where L and W denote the length and width of the conduction channel between source and drain electrodes 403, respectively,  $C_i$  denotes the capacitance per unit area of the dielectric (i.e.  $\text{SiO}_2$ , in the present embodiment) and  $dI_{sd}/dV_{sd}$  represents the slope of the linear region in the transfer plot.

10 In the arrangement of Figure 4, the electrodes 403 interface with the portions 105 of the TMD 101 which are surface modified, i.e. they are in direct electrical contact with these portions. However, the majority of the channel remains unmodified.

This arrangement therefore provides a field effect transistor based on the semi-  
 15 conductor behaviour of the TMD, while simultaneously ensuring that the source and drain electrodes are in direct electrical contact with metallic portions of the TMD, thereby ensuring Ohmic contact between the with low contact resistance and avoiding a Schottky barrier at the contact between the electrodes and the semiconducting material.

Thus, the alkali metal functionalization described above according to embodiments, particularly functionalization using Caesium and/or Rubidium, provides a simple method of achieving a high-performance transistor with high mobility, high current on/off ratio, low subthreshold swing. The device of Figure 4 therefore is a high-quality  
5 device which has a fast on/off speed and is cost-efficient.

Figure 5 shows a sandwich framework FET according to an embodiment of the invention.

10 As in the embodiment of Figure 4, the transistor 5 comprises a mono-layer of TMD 101 with source and drain electrodes 403 provided on the substrate 401 at either end of the TMD layer 101 and a layer of photoresist material 405 arranged on a portion the surface of the TMD layer 101. In the embodiment of Figure 5, the photoresist 405 is PMMA, however, the person skilled in the art will appreciate that other materials  
15 could be employed according to embodiments. In embodiments, the photoresist or other insulating layer 405 may be omitted partially or completely.

The TMD and source and drain electrodes are arranged on a dielectric layer 501. In the embodiment of Figure 5, the dielectric layer comprises a sheet of hexagonal boron  
20 nitride (h-BN). However, the person skilled in the art will appreciate that other dielectric layers may be employed according to embodiments.

In an embodiment, the thickness of the dielectric layer 501 (in this embodiment, h-BN) may particularly be in the range 10-20nm. Thinner dielectric layers may induce undesirable quantum tunnelling into the device.

5

The dielectric layer is arranged on a bottom gate electrode layer 503. In the embodiment of Figure 5, the bottom gate electrode comprises a layer of Graphene.

The skilled person will appreciate that other suitable materials may be employed according to embodiments. In an embodiment, the thickness of the bottom gate

10 electrode layer may particularly be less than 10nm.

The sandwich arrangement described above is arranged on a silicon-based substrate 401 as described above in relation to the embodiment of Figure 4.

15 As in the embodiment of Figure 4 a layer of alkali metal is present on the portions 105 of the surface of the TMD at either end of the TMD layer 101 which are not covered by the photoresist 405. The TMD layer 101 is therefore surface modified at each end 105 but is unmodified in its central portion 107.

In an embodiment, the width of each of the portions 105 of the TMD layer on which alkali metal is present (i.e. the distance from the electrodes 403 from which these portions extend) is in the range 0.2-5  $\mu\text{m}$ . In an embodiment, they have a width in the range 0.2-0.3  $\mu\text{m}$ .

5

In an embodiment, the alkali metal layer employed in the embodiment of Figure 5 comprises Caesium and/or Rubidium.

In the embodiment of Figure 5, the TMD may be selected from  $\text{MoS}_2$ ,  $\text{WS}_2$ ,  $\text{MoSe}_2$  and  
10  $\text{WSe}_2$ ,  $\text{MoTe}_2$ , alkali metal-doped  $\text{MoTe}_2$ , alkali metal-doped  $\text{MoSe}_2$ , alkali metal-doped  $\text{MoS}_2$ , alkali metal-doped  $\text{WSe}_2$ , and alkali metal-doped  $\text{WS}_2$ .

In particular, the TMD may be selected from  $\text{WSe}_2$  and  $\text{MoTe}_2$ . More particularly, the TMD may be  $\text{WSe}_2$ .

15

As explained above, beyond a certain thickness of alkali metal, the TMD layer may be metallic at each end 105 but behave as a semiconductor towards the centre of the layer 107, in the region 107 positioned under the photoresist 405. In the embodiment of Figure 5, the TMD is employed as a n-type unipolar semiconductor. In an  
20 embodiment, the TMD has a 1T or 1T' phase at each end 105 adjacent to the source

and drain electrodes 403 and a 2H phase in the portion 107 beneath the photoresist 405 which is not surface modified with alkali metal. The TMD is therefore comprises a hetero-phase contact 111 and the device 5 is therefore a hetero-phase transistor.

- 5 In an embodiment, the thickness of the alkali metal lies in the range 0.2nm to 5nm. In an embodiment, the thickness of the alkali metal lies in the range 0.4nm to 2nm. In an embodiment, the thickness of the alkali metal is approximately 1.0nm.

In an embodiment, the thickness of the alkali metal is chosen according to the desired  
10 properties of the device.

In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the thickness of the alkali metal is such that there is ohmic contact between the electrodes and the TMD layer.

15

In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the thickness of the alkali metal is such that the current on/off ratio at room temperature (298K) of the device 5 is at least  $10^7$ , in particular in the range from  $10^7$  to  $10^9$ .

The current on/off ratio of the device is defined by the ratio of the on state current and off state current, i.e. it is the ratio of the current maximum and the current minimum in the transfer characteristic curve.

- 5 In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the thickness of the alkali metal is such that the field effect electron mobility in the surface modified portions of the TMD is at least  $70 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ .

The field effect electron mobility  $\mu$  of the device is derived from the linear regime of a  
10 transfer plot of current between source and drain electrodes ( $I_{sd}$ ) against potential difference across the source and drain electrodes ( $V_{sd}$ ) using the equation:

$$\mu = \frac{L}{WC_i V_{sd}} \frac{dI_{sd}}{dV_{sd}}$$

where L and W denote the length and width of the conduction channel between source and drain electrodes 403, respectively,  $C_i$  denotes the capacitance per unit area  
15 of the dielectric 501 (i.e. BN in the embodiment of Figure 5) and  $dI_{sd}/dV_{sd}$  represents the slope of the linear region in the transfer plot.

In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the thickness of the alkali metal is chosen such that subthreshold swing is less than  $85 \text{ mV}$   
20  $\text{dec}^{-1}$ , particularly in the range  $60$  to  $85 \text{ mV dec}^{-1}$ .

The subthreshold swing of the device is determined from  $dV_g/d(\log I_{sd})$ , where  $V_g$  is the gate voltage and  $I_{sd}$  is the current between source and drain electrodes.

- 5     Figure 6 shows a transistor-based logic inverter according to an embodiment. The device comprises a back-gate electrode 503 providing the input signal ( $V_{IN}$ ) and a dielectric layer 501 arranged on a substrate 401 as described in association with the device of Figure 4.
- 10    The device further comprises three parallel electrodes 605, 607, 609 arranged on the dielectric layer 501, serving as the power supply (VDD; 605), output signal (VOUT; 607), and ground (GND; 609), respectively, between which a layer of TMD 101 forms two channels 601 and 603 in series.
- 15    A Photoresist 405 is arranged to completely cover the TMD of one channel, 601 such that no surface modification of the TMD is present in this channel therefore enabling this channel to retain the p-type dominated ambipolar behaviour of the TMD.
- 20    In contrast, the other channel 603 is only partially covered by the PMMA photoresist 405 with alkali-metal surface modification at each end, adjacent to the corresponding

electrodes 605. Thus, this channel behaves as an n-type transistor as described above in relation to Figures 4 and 5.

In embodiments, the photoresist layers 405 may be completely or partially omitted  
5 from either or both of the channels.

Thus, the embodiment of Figure 6 corresponds to a TMD inverter with two channels in series. Through spatially controlling the exposed regions near the metal electrodes of one TMD channel, unipolar hetero-phase n-type transistor can be obtained. In  
10 contrast, another channel is fully covered by the PMMA photoresist, where the p-type dominated ambipolar transport behaviour is retained. In the embodiment of Figure 6, multilayer h-BN and graphene are used as the dielectric layer and bottom gate electrode, respectively, however the skilled person will appreciate that other suitable materials could be employed according to embodiments. The graphene provides the  
15 input signal ( $V_{IN}$ ), and the three parallel electrodes on the TMD flake serve as the power supply ( $V_{DD}$ ), output signal ( $V_{OUT}$ ), and ground (GND), respectively.

In an embodiment, the thickness of the alkali metal layer is chosen according to the desired properties of the n-type channel.

In an embodiment, the thickness of the alkali metal is in the range 0.2nm to 5nm, particularly 0.4nm to 2nm. In an embodiment, the thickness of the alkali metal is approximately 1.0nm.

- 5 In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the thickness of the alkali metal may be such that the gain ( $-dV_{OUT}/dV_{IN}$ ) achievable by the inverter 6 is greater than 100 when  $V_{DD} = 2.5$  V.

- In an embodiment, the alkali metal comprises Caesium and/or Rubidium and the  
10 thickness of the alkali metal may be such that that inverter can achieve a gain greater than 5 for a static power consumption (defined as  $P = V_{DD} \times I_{DD}$ ) of less than 10 pW when  $V_{DD} = 0.5$  V.

- As shown below, experimental results have shown that inverters according to this  
15 embodiment have high voltage gain, thereby enabling fast logic state inversion, high accuracy and low power consumption.

- Although the integration of materials according to the embodiment of Figure 1 have been described in relation to three devices 4, 5 and 6 according to embodiments, the  
20 person skilled in the art will understand that these devices are merely intended to be

representational of the potential application of materials according to embodiments. Indeed, materials according to embodiments described above are extremely flexible and compatible with various device structures. They can be applied to almost all electronic and optoelectronic devices to improve charge injection/collection efficiency.

- 5 The thickness of the alkali metal layer may be varied in order to fine-tune the electrical properties of the material according to its intended implementation.

Figure 7 shows a method of producing the material of Figure 1 according to an embodiment. It is also suitable for producing the relevant layers in the devices in  
10 Figures 4, 5 and 6.

In step S701 the TMD 101 is provided. The layer may be a monolayer, a bilayer, or comprise three or more layers according requirements of the final material. Bulk TMD crystals are commercially available, for example from HQ-Graphene. Monolayer and  
15 bilayer TMD can be produced from bulk TMD via, for example, mechanical exfoliation using Scotch tape.

In an embodiment, the TMD may be transferred to a suitable substrate such as Silicon dioxide prior to performing step S703. In an embodiment, electrodes may be  
20 patterned onto the TMD using electron beam lithography prior to performing step

S703. Thus, steps S703 to S707 may be performed *in situ* in an electronic device, such as those described above in relation to Figures 4, 5 and 6.

If electrode patterning is performed, after patterning the source and drain electrodes  
5 on the TMD, the electrodes may be thermally evaporated onto the substrate, for example by thermally evaporating Pd and/or Au. Excess metal may then be removed from the sample, for example by soaking in acetone according to procedures well known in the art. The method then proceeds to step S703.

10 In step S703 the surface 109 of the TMD layer is coated with a barrier layer 405 of photoresist such as PMMA. In an embodiment, the barrier layer is applied to the TMD layer using spin-coating.

In step S705, electron beam lithography (EBL) is employed to remove the photoresist  
15 on the portions 105 of the TMD layer to be surface modified. In the embodiment of Figure S705, these are the portions at the edge of the layer.

In step S707 a layer of one or more alkali metals 103 is evaporated directly onto the TMD layer. In an embodiment, this is done under vacuum from one or more alkali  
20 metal getters. Suitable getters are commercially available, for example from SAES. In

an embodiment, the one or more alkali metals comprise Caesium and/or Rubidium and a layer of Caesium and/or Rubidium is evaporated onto the TMD layer from, for example, a Caesium and/or Rubidium getter.

- 5 In an embodiment, the alkali metal getter is heated in a high-vacuum chamber with the TMD in order to achieve evaporation of the alkali metal onto the exposed surfaces of the TMD. Evaporation of the alkali metal from the getter may be achieved, for example by supplying a DC current to a feedthrough into the vacuum chamber.
- 10 In an embodiment, the vacuum chamber should be under a high vacuum condition of less than  $10^{-7}$  mbar. Such pressures can be achieved by pumping a suitable chamber with a turbopump. Turbopumps suitable for achieving a high vacuum are commercially available, for example from Pfeiffer Vacuum GmbH. Components for a chamber suitable for supporting such a vacuum are also commercially available, for example,  
15 from UHV Design.

Due to the presence of the photoresist 405 acting as a barrier layer, film growth of the alkali metal is restricted to the exposed portions 105 and 105 of the TMD layer.

The thickness of the alkali metal can be monitored by monitoring the weight of the material during evaporation, for example using a quartz crystal microbalance (QCM), thereby enabling it to be controlled according to the desired properties of the material or device, as appropriate.

5

Quartz crystal microbalances (and corresponding feedthroughs) suitable for use in accordance with embodiments are commercially available, for example from Testbourne Ltd.

- 10 In an embodiment, the vacuum chamber is configured such that the QCM is positioned so as to protect the sample from alkali metal deposition while the evaporation rate from the alkali metal getter is brought to required levels. Once it achieves the desired rate, the QCM is moved out of the way in order to enable alkali metal deposition. Once the desired evaporation onto the sample is complete, the QCM is moved back into
- 15 position to protect the sample from further deposition.

A suitable *in situ* vacuum characterization system for use in accordance with embodiments is given in Lei, B., et al. (2017). *Nano Research*, 10(4), 1282-1291.

The photoresist layer may or may not be removed following the application, according to desired use.

Thus, the method of Figure 7 provides a method of producing the materials and  
5 devices according to embodiments which may be performed in situ and easily  
integrated with conventional CMOS processes, thereby enabling straightforward  
integration into the fabrication process. This method provides an effective, damage-  
free and non-volatile procedure for realizing phase transitions in TMDs such as WSe<sub>2</sub>.

## 10 Examples

Selected advantageous physical properties of the above described embodiments will  
now be described in accordance with the following non-limiting examples.

### 15 **Fabrication of Pristine 2D WSe<sub>2</sub> transistor**

Scotch tape was used to mechanically exfoliate WSe<sub>2</sub> flakes from bulk WSe<sub>2</sub> crystals  
(commercially obtained from HQ-graphene), and then quickly transferred onto a  
degenerately p-type doped silicon substrate with 300 nm SiO<sub>2</sub>. Monolayer and bilayer

20 WSe<sub>2</sub> were found by utilizing a high-resolution optical microscope (Nikon Eclipse

LV100D), and further confirmed by AFM and Raman measurements.

Polymethylmethacrylate (PMMA) photoresist (commercially obtained from MicroChem) was subsequently spin coated on the silicon substrate for the conventional e-beam lithography (EBL) process. After patterning the source and drain electrodes on WSe<sub>2</sub>, 5 nm Pd and 60 nm Au were thermally evaporated onto the substrate. The sample was then soaked in acetone for about 1 hour to lift off excess metal.

Figures 8a-c show results for the bilayer WSe<sub>2</sub> device, where the WSe<sub>2</sub> flakes were mechanically exfoliated onto a degenerately p-type doped silicon wafer with a 300 nm SiO<sub>2</sub> layer. Standard lithography was then carried out to define the WSe<sub>2</sub> channel followed by the metal deposition of Pd/Au. Fig. 8a shows the line profile derived from the Atomic Force Microscope (AFM) image of the device. It reveals that the thickness of the WSe<sub>2</sub> flake is around ~1.7 nm, indicating its bilayer nature. Raman and photoluminescence (PL) measurements (Figures 8b and 8c, respectively) were employed for further verification. Three Raman characteristic peaks located at 250 cm<sup>-1</sup> (E<sub>12g</sub>), 257.5 cm<sup>-1</sup> (A<sub>1g</sub>) and 309 cm<sup>-1</sup> (B<sub>12g</sub>), and the PL spectrum 801 exhibits the direct bandgap emission peak 803 at ~1.64 eV and the indirect bandgap emission peak 805 at ~1.57 eV, further confirming the bilayer nature of the WSe<sub>2</sub> flake.

20

#### Surface modification with Cs

In order to investigate the Cs modification induced phase transition in bilayer WSe<sub>2</sub> via in situ electrical measurement, the pristine WSe<sub>2</sub> device was wire bonded onto a lead chip carrier and loaded into a home-made high vacuum system ( $\sim 10^{-7}$  mbar) with in situ film growth and cryogenic electrical measurements capabilities. The vacuum  
5 system was fabricated in accordance with the design given in Lei, B., et al. (2017), Nano Research, 10(4), 1282-1291.

An Agilent 2912A precision source/measure unit (SMU) was utilized to perform the related electrical measurements. Caesium was evaporated in situ from a SAES Getter  
10 directly to the devices and a quartz crystal microbalance (QCM) (commercially obtained from Testbourne Ltd) was employed to calibrate the nominal thickness. The temperature dependent experiments described below were conducted on a cryogenic stage with liquid nitrogen for sample cooling.

15 The sample was loaded onto the sample stage through a flexible fast entry door. After several hours' pumping, the sample was pulled back to a particular position for in situ deposition, where a thermal effusion cell was equipped to evaporate dopant. The quartz crystal microbalance (QCM) was placed in front of the sample stage to precisely monitor the deposition rate. Once the Cs evaporate rate was confirmed, the QCM was  
20 shifted upwards to allow Cs to deposit onto the sample. After the evaporation, the

QCM was shifted downward to block Cs. The Cs was evaporated via a DC current (3.8 A) provided through a feedthrough.

Figure 9a shows a schematic representation of the bilayer WSe<sub>2</sub> device in a FET structure with Pd/Au (5nm/60 nm) as the metal contacts 921 and 300 nm SiO<sub>2</sub> layer as the dielectric.

Figure 9b and Figure 9c show the transport characteristics ( $I_{sd}$ - $V_g$ ) of the pristine bilayer WSe<sub>2</sub> FET in high vacuum condition ( $10^{-7}$  mbar). The results clearly reveal a hole-dominated ambipolar transport behaviour, where gate voltage sweeps from -80 V to 50 V under a fixed bias ( $V_{sd} = 1$  V).

Figure 9d shows Transfer characteristic evolution of the WSe<sub>2</sub> FET as a function of Cs thickness following in situ deposition of Cs on the device as described above. The thicknesses shown are 0nm (901), 0.01nm (903), 0.07nm (905), 0.19nm (907), 0.4nm (909) and 1.0 nm (911). Two distinct stages can be observed, including i) a significant n-type doping stage with strongly enhanced on-current in the electron transport regime under the low Cs doping level (Cs nominal thickness < 0.2 nm); and ii) the WSe<sub>2</sub> device exhibits a nearly gate independent transport behaviour when the Cs nominal thickness is above 0.4 nm, indicating a semiconductor to metal phase transition.

Figure 9e shows the electrical conductance ( $G$ ) versus Cs thickness at  $V_g = 0$  V. The electrical conductance ( $G = I_{sd}/V_{sd}$ ) under  $V_g = 0$  V is remarkably enhanced by nearly 7 orders of magnitude, from  $2.1 \times 10^{-11}$  S to  $1.1 \times 10^{-4}$  S after 1.0 nm Cs decoration.

- 5 Figure 9f shows output curves ( $I_{sd}-V_{sd}$ ) for the pristine (915) and 1.0 nm (913) Cs-modified WSe<sub>2</sub> FET at different gate voltage,  $V_g$ , from 0 to 50 V. As shown in the output curves of the WSe<sub>2</sub> device before and after 1.0 nm Cs modification, the pristine WSe<sub>2</sub> device exhibits a Schottky contact behaviour, while ohmic contact feature is identified after 1.0 nm Cs decoration. The large enhancement of  $I_{sd}$  reveals the reduction of
- 10 contact and channel resistances, originating from the semiconductor to metal phase transition.

The semiconductor to metal phase transition in the bilayer WSe<sub>2</sub> device was further characterised by temperature-dependent transport measurements. The temperature

15 dependent experiments were conducted on a cryogenic stage with liquid nitrogen for sample cooling and the results are shown in Figures 9g and 9h in which the evolution of the electrical conductance for both pristine (917) and Cs-modified (919) bilayer WSe<sub>2</sub> device as a function of temperature with the gate voltages of (Figure 9g)  $V_g = -80$  V and (Figure 9h) 50 V.

As can be seen from Figures 9g and 9h, the semiconducting and metallic phased bilayer WSe<sub>2</sub> devices present opposite evolution trends as a function of temperature. For the pristine semiconducting WSe<sub>2</sub> device, the electrical conductance gradually rises with the increase of temperature, originating from the dramatical enhancement of thermally activated carriers. In contrast, increasing temperature in 1.0 nm Cs-modified metallic WSe<sub>2</sub> device leads to the decrease of the electrical conductance. High temperature enhances the electron scattering in the metallic WSe<sub>2</sub>, resulting in the reduction of electrical conductance.

Figure 9i shows the electrical conductance evolution of the bilayer WSe<sub>2</sub> device after 1.0 nm Cs functionalization with respect to temperature at different V<sub>g</sub> from -80 V to 50 V. The conductance progressively decreases as the temperature increases under all gate voltages, clearly revealing the metallic feature of the Cs-modified WSe<sub>2</sub> flake and further corroborating the semiconductor to metal phase transition induced by Cs surface functionalization.

To understand the semiconductor to metal phase transition mechanism for Cs-modified WSe<sub>2</sub>, in situ XPS/UPS experiments were further employed. In situ UPS and XPS measurements on Cs surface-modified bulk WSe<sub>2</sub> (obtained from HQ-graphene) were carried out in an ultrahigh vacuum chamber (base pressure  $\sim 10^{-10}$  mbar). He I (21.2 eV) was utilized as the excitation source and a sample bias voltage of 5 V was

applied for UPS characterization. Al K $\alpha$  (148.7 eV) served as the excitation source for XPS measurements. The nominal thickness of in situ deposited Cs layers was estimated by monitoring the attenuation of WSe<sub>2</sub> core level peaks and further calibrated by QCM. The results are shown in Figure 10 in which Figure 10 (a) shows UPS spectra evolution at low kinetic energy region, Figure 10(b) shows XPS core level spectra of W 4f as a function of Cs thickness on WSe<sub>2</sub>; Figure 10(c) shows XPS core level spectra of Se 3d as a function of Cs thickness on WSe<sub>2</sub> and Figure 10(d) shows UPS valence band spectra near the Fermi level region. Pristine WSe<sub>2</sub> is denoted by 1001, 0.01nm Cs by 1003, 0.10nm Cs by 1005, 0.20nm Cs by 1007, 0.40nm Cs by 1009, and 1.00nm Cs by 1011 in all figures. Here  $\phi$  denotes the work function and  $\Delta E$  denotes the energy difference.

The work function (WF) of the pristine WSe<sub>2</sub> is measured to be  $\sim 4.02$  eV, which sharply dropped to  $\sim 2.2$  eV after 1.0 nm Cs decoration. The decrease of WF implies the significant electron transfer from Cs to WSe<sub>2</sub> at the Cs/WSe<sub>2</sub> interface, resulting from the ultralow WF of Cs ( $\sim 2.14$  eV).

Figures 10(b) and 10(c) show the evolution of W 4f and Se 3d core level binding energy as a function of Cs thickness, respectively. As increasing the Cs deposition thickness to 0.2 nm, the electron doping effect of Cs on WSe<sub>2</sub> makes the Fermi level of WSe<sub>2</sub> move towards its conduction band and hence the binding energy of W 4f and Se 3d slightly increases by 0.1 eV and 0.15 eV, respectively. Intriguingly, when the Cs thickness

increases from 0.2 nm to 1.0 nm, the W 4f and Se 3d core levels move towards the lower binding energy by  $\sim 0.3$  eV and  $\sim 0.35$  eV, respectively. This is consistent with previous reports of K-functionalization and hence electron-doping induced semiconductor to metal (2H to 1T') phase transition in bilayer WSe<sub>2</sub>. Further Cs

5 deposition leads to the accumulated negative charge on the metallic WSe<sub>2</sub> surface and hence the core level peaks move towards the lower binding energy.

The valence band spectra shown in Figure 10(d) can further validate the metallization of the heavily doped WSe<sub>2</sub>. At low surface modification levels (Cs thickness  $< 0.4$  nm), a

10 downward band bending of the valence band is observed due to the electron doping. When the Cs thickness is above 0.4 nm, a sharp peak emerges around the Fermi level, clearly revealing the metal-like features, further confirming the semiconductor to metal phase transition.

15 Figure 11a shows the Photoluminescence (PL) spectra for the bilayer WSe<sub>2</sub> flake before (1103) and after 0.1 nm Cs modification (1101). Figure 11b shows the Raman spectra of the pristine, 0.1 nm and 1.0 nm Cs-modified WSe<sub>2</sub>. Among the three polymorphs in WSe<sub>2</sub>, both 1T and 1T' are metallic. Previous reports suggest that the 1T phase of group VI TMDs is unstable and spontaneously transforms to 1T' phase with energy

20 relaxation. Therefore, without wishing to be bound by theory, it is proposed that the metallic phase of the WSe<sub>2</sub> after Cs doping is 1T'. In situ Raman and PL were carried

out to reveal the phase transition of Cs-modified WSe<sub>2</sub> and the results of Figure 11a and 11b show in situ PL and Raman spectra, respectively, of the bilayer WSe<sub>2</sub> before and after Cs deposition. Upon 0.1 nm Cs deposition, the PL peak for bilayer WSe<sub>2</sub> is immediately quenched due to the significant charge transfer. Pristine bilayer WSe<sub>2</sub> shows three characteristic peaks in the Raman spectrum located at 250 cm<sup>-1</sup> (E<sub>2g</sub><sup>1</sup>), 257.5 cm<sup>-1</sup> (A<sub>1g</sub>) and 309 cm<sup>-1</sup> (B<sub>2g</sub><sup>1</sup>) respectively. After 0.1 nm Cs coverage, the intensity of these peaks is largely reduced. Further increasing the Cs thickness to 1.0 nm leads to the phase transition of the bilayer WSe<sub>2</sub> from the semiconducting 2H phase to 1T' metallic phase. The B<sub>2g</sub><sup>1</sup> peak totally vanishes, and five new peaks emerge in the low wavenumber regime, at around ~93, 114, 227, 242 and 260 cm<sup>-1</sup>. These new peaks correspond to the characteristic peaks of the WSe<sub>2</sub> in 1T' phase. Therefore, without wishing to be bound by theory, the phase transition of Cs-modified WSe<sub>2</sub> observed here can be assigned to a 2H to 1T' phase transition.

## 15 Hetero-phase device fabrication

For heterophase device fabrication according to the embodiment of Figure 4, the pristine WSe<sub>2</sub> device was first fabricated in accordance with the method described above. In order to realize the partially surface-modified device, PMMA photoresist was spin-coated again and a second EBL process was performed to expose desired area around the contact after the lift off of the excess metal. The device was then loaded

into a vacuum system as previously described for Caesium evaporation for electrical characterization.

Fig. 12a exhibits the evolution of the transfer characteristics as a function of Cs thickness, with thicknesses of 0nm (1301), 0.05nm (1303), 0.20nm (1305), 0.50nm (1307) and 1.00nm (1309). As discussed before, the WSe<sub>2</sub> flake is n-type doped at low Cs deposition level. Further increasing Cs thickness to a high level induces the phase transition in the exposed region, leading to the 1T' contact. The saturation current with 1T' phase contact is approximately 2 orders of magnitude higher than that of the pristine device with Pd contact, leading to a giant gate modulation effect as well as a high current on/off ratio of  $\sim 10^7$ .

The field-effect electron mobility is also dramatically improved from 0.6 to 37.7 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> as shown in Figure 12b, which shows the evolution of the electron mobility versus Cs thickness. This indicates the superior transport property of the device with 1T' contact.

Figures 12c and Figure 12d illustrate the output curves of the device under gate voltages 0V (1311), 20V (1313), 40V (1315) and 50V (1317) before (Figure 12d) and after (Figure 12c) 1.0 nm Cs functionalization. The pristine transistor exhibits a clear Schottky contact behaviour, whereas an ideal ohmic contact can be observed after Cs

functionalization, as reflected by the symmetric and linear feature of the output curves.

Thus, *In situ* Cs surface modification has been demonstrated as an effective approach  
5 to induce the semiconducting to metallic phase transition in 2H WSe<sub>2</sub>, which offers the opportunity to realize high performance 2H-1T' hetero-phase WSe<sub>2</sub> transistor via spatially controlling the phase transition region.

The Schottky barrier height of the hetero-phase transistor was further investigated,  
10 and the results are shown in Figure 13a as a function of gate voltage  $V_g$ . According to Figure 13a, the SB in the hetero-phase transistor is determined to be as low as ~9.4 meV for the electron-transport. Such negligible SB can significantly enhance the electron injection into the semiconductor, resulting in true Ohmic contact behaviour under high electrostatic doping.

15

To further quantify the contact quality of the ideal n-type hetero-phase WSe<sub>2</sub> transistor, the width normalized contact resistance ( $R_c$ ) was extracted via the transfer length method (TLM). A series of WSe<sub>2</sub> (5-layer) transistors with different channel lengths were employed for the measurement. To ensure accuracy, it was assumed that  
20 the channel segments covered by the metal contact have no contribution to the overall channel length. Moreover, since one of the Schottky contacts can easily

become forward-biased when applying high bias voltage, a very small bias ( $\sim 10$  mV) was employed in order to avoid an underestimation of the  $R_c$ . Figure 13b shows the width-normalized total resistance ( $R_{tot}$ ) as a function of the channel length at  $V_g = 5$  V. The  $R_{tot}$  is linearly fitted, where the y intercept yields the total contact resistance ( $2R_c$ ) and the slope represents the sheet resistance ( $R_{sh}$ ) of the channel. A low contact resistance of  $\sim 4.3$  k $\Omega$   $\mu$ m is obtained at  $V_g = 5$  V, which can be attributed to the combined effects of the SB height lowering and the SB width narrowing.

To fabricate a sandwich framework device, according to the embodiment of Figure 5, few-layer graphene (commercially obtained from HQ-Graphene) was firstly exfoliated on a SiO<sub>2</sub>/Si substrate via scotch tape. Then 15 nm-thick hexagonal boron nitride (n-BN) (commercially obtained from ACS Material, LLC) and WSe<sub>2</sub> (commercially obtained from HQ-graphene) were subsequently exfoliated on a viscoelastic stamp using polydimethylsiloxane (PDMS) (commercially obtained from the Merck Group) and transferred onto the desired graphene flake. The procedures described above were employed to obtain a contact exposure channel to achieve the 2H-1T' hetero-phase FET. The device was then loaded into a high vacuum chamber for further measurements.

Figure 14a shows the transfer characteristic evolution of the device as a function of Cs thickness. Results for Cs thicknesses of 0.0nm (1401), 0.01nm (1403), 0.08nm (1405), 0.20nm (1407) and 1.00nm (1409) are shown.

- 5 Low-level Cs deposition induces an electron-doping effect in the uncovered WSe<sub>2</sub>. Further increasing the Cs thickness leads to the phase transition of the uncovered WSe<sub>2</sub>, and hence the realization of 2H-1T' contact. It is worth noting that the on current of the 2H-1T' hetero-phase device is approximately 3 orders of magnitude higher than that of the pristine device with Pd contact, leading to an ultrahigh current
- 10 on/off ratio  $\sim 10^8$ . In addition, the subthreshold swing (SS) defined as  $dV_g/d(\log I_{sd})$  is optimized to 75 mV dec<sup>-1</sup>, which is close to the theoretical limit of 60 mV dec<sup>-1</sup>. The field-effect mobility can be extracted from the linear regime of the transfer curve by using the equation:

$$\mu = \frac{L}{WC_i V_{sd}} \frac{dI_{sd}}{dV_{sd}}$$

15

where L and W denote the length and width of the conduction channel, respectively, C<sub>i</sub> denotes the capacitance per unit area of the dielectric and  $dI_{sd}/dV_{sd}$  represents the slope of the linear region in the transfer plot.

Figure 14b shows the corresponding electron mobility versus Cs thickness. The electron mobility is significantly enhanced from  $1.33 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  to  $70 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  by nearly 50 times.

5 Figures 14c and 14d show output curves for the device before (Figure 14c) and after 1.0 nm (Figure 14d) Cs contact doping at different gate voltages 0V (1415), 1V (1417), 2V (1419), 3V (1421), 4V (1423) and 5V (1425). The output curves of the pristine WSe<sub>2</sub> device are nonlinear even at a high electrostatically doping level ( $V_g \sim 5\text{V}$ ), illustrating a clear Schottky contact behaviour. After 1.0 nm Cs modification, the current is largely  
10 improved by over 2 orders of magnitude at each gate voltage. Moreover, the output curves are almost linear especially at the low  $V_{sd}$  regime, suggesting a nearly-ideal ohmic contact.

A second sandwich framework device according to the embodiment of Figure 5, was  
15 fabricated in accordance with the same procedure described above. Figure 14e shows the transfer characteristic evolution as a function of Cs thickness for this second device. Results for Cs thicknesses of 0.0nm (i.e. pristine WSe<sub>2</sub>; 1413) and 1.00nm (1411) are shown.

20 The current on/off ratio of the Cs doped device was found to be even higher at  $\sim 10^9$ . In addition, the subthreshold swing (SS) defined was measured to be  $61 \text{ mV dec}^{-1}$ .

A device according to the embodiment of Figure 6 was fabricated as described above with regard to the FET sandwich device but modified to obtain a contact exposure channel and a full PMMA covered channel. As before, the device was loaded into a  
5 high vacuum chamber for further measurements.

Figure 15a shows transfer characteristics for N-FET 1501 and P-FET 1503 demonstrating that unipolar hetero-phase n-type transistor can be obtained through spatially controlling the exposed regions near the metal electrodes of one WSe<sub>2</sub>  
10 channel, while p-type dominated ambipolar transport behaviour is retained in the other channel which is fully covered by the PMMA photoresist.

Figure 15b shows the output characteristics of the homogeneous WSe<sub>2</sub> inverter as a function of  $V_{IN}$  at  $V_{DD} = 1\text{ V}$  (1505),  $2\text{ V}$  (1507), and  $2.5\text{ V}$  (1509) respectively. By  
15 sweeping the input voltage from  $-1\text{ V}$  to  $2\text{ V}$ , the inverter experiences a 'high state' (high  $V_{OUT}$ ), 'steep slope' (sharp decrease of  $V_{OUT}$ ), and a 'low state' (low  $V_{OUT}$ ) sequentially. One key parameter to evaluate the performance of the inverter is the voltage gain defined by the slope of output characteristics ( $\text{gain} = -dV_{OUT}/dV_{IN}$ ). This is further shown in Figure 16 (a) which shows the output characteristics as a function of  
20  $V_{IN}$  at  $V_{DD} = 0.5\text{ V}$  (1601),  $1.0\text{ V}$  (1603),  $1.5\text{ V}$  (1605),  $2.0\text{ V}$  (1607) and  $2.5\text{ V}$  (1609).

Figure 15c shows the extracted gain as a function of  $V_{IN}$  at three different  $V_{DD}$  (reference numerals as above). At small  $V_{DD}$  of 1 V, the gain is around 13. By increasing the  $V_{DD}$  to 2 V and 2.5 V, the gain can reach up to 49 and 106, respectively. It is noted that these gains are the highest among all 2D-material-based homo-inverters. Without  
5 wishing to be bound by theory, it is proposed that such high gain is mainly attributed to the low SS ( $\sim 75$  mV dec<sup>-1</sup>) and ultrahigh current on/off ratio ( $\sim 10^8$ ) of the Cs-modified WSe<sub>2</sub> transistor, which ensure the fast switching between the 'high state' and the 'low state' of the inverter.

10 Figure 15d shows the evolution of the power consumption of the device versus  $V_{DD}$  from 0.5 V to 2.5 V. The power is around 280 nW at  $V_{DD} = 2.5$  V, which progressively decreases to an ultralow value of  $\sim 5$  pW at  $V_{DD} = 0.5$  V. It is worth noting that the gain at  $V_{DD} = 0.5$  V can be maintained at a proper level of around 8 which is highly competitive among all 2D-material-based logic inverters for such an ultralow power  
15 consumption. This is shown in Figure 16(b) which shows the output curve (1611) and corresponding voltage gain (1613) as a function of  $V_{IN}$  at  $V_{DD} = 0.5$  V.

The results above show the realisation of a semiconducting-to-metallic (2H to 1T') phase transition in WSe<sub>2</sub> via in situ Cs surface functionalization. The phase transition is  
20 firstly revealed by the in situ electrical characterization of the WSe<sub>2</sub> FET. The Cs-functionalized WSe<sub>2</sub> transistor exhibits gate-independent transport behaviour with

nearly 7 orders of magnitude enhancement in electrical conductance. As revealed by the in-situ UPS/XPS and Raman measurements, the 2H to 1T' phase transition originates from the giant electron doping from Cs to WSe<sub>2</sub>. By implementing the 1T' phase WSe<sub>2</sub> so formed as the contact electrodes, a 2H-1T' hetero-phase WSe<sub>2</sub> transistor is obtained with remarkably enhanced field-effect electron mobility, increased by nearly 50 times, reaching up to  $\sim 70 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ . Moreover, the device demonstrates an ultrahigh current on/off ratio  $\sim 10^8$  and low SS  $\sim 75 \text{ mV dec}^{-1}$ , enabling the realization of high performance WSe<sub>2</sub> logic inverter with ultralow power consumption of  $\sim 5 \text{ pW}$  and a high voltage gain of  $\sim 106$ , higher than all the 2D-material-based homo-inverters.

Although the above results were obtained under vacuum, the skilled person will appreciate that any environment that excludes oxygen and water could equivalently have been employed, such as a substantially 100% N<sub>2</sub> or otherwise inert environment under normal atmospheric conditions.

Thus, alkali metal functionalization induced phase transition, particularly Cs metal functionalization induce phase transition in TMDs provides a simple method to achieve high performance TMD hetero-phase transistor and logic inverter.

In particular, in situ alkali-metal surface modification, particularly in situ Cs surface modification, has been demonstrated as an effective approach to induce the semiconducting to metallic phase transition in 2H TMDs, which offers the opportunity to realize a high performance 2H-1T' hetero-phase TMD transistor via spatially  
5 controlling the phase transition region.

In the foregoing detailed description, embodiments of the present disclosure in relation to a transition metal dichalcogenide and devices thereof are described with reference to the provided figures. The description of the various embodiments herein  
10 is not intended to call out or be limited only to specific or particular representations of the present disclosure, but merely to illustrate non-limiting examples of the present disclosure. The present disclosure serves to address at least one of the mentioned problems and issues associated with the prior art. Although only some embodiments of the present disclosure are disclosed herein, it will be apparent to a person having  
15 ordinary skill in the art in view of this disclosure that a variety of changes and/or modifications can be made to the disclosed embodiments without departing from the scope of the present disclosure. Therefore, the scope of the disclosure as well as the scope of the following claims is not limited to embodiments described herein.

20 Further embodiments are given in the following statements:

1. A transition metal dichalcogenide (TMD) including a first portion, wherein the

first portion is surface modified with a Group 1 alkali metal.

2. The TMD of 1, wherein the Group 1 alkali metal forms a layer on a side of the first portion.

3. The TMD of 1 or 2, wherein the Group 1 alkali metal is selected from lithium,

5 sodium, potassium, rubidium, caesium or francium.

4. The TMD of any of 1 to 3, further including a second portion, wherein the first portion has a different phase structure to the second portion.

5. The TMD of any of 1 to 4, wherein the first portion has a metallic octahedral (1T') phase structure.

10 6. The TMD of any of 1 to 5, wherein a thickness of the Group 1 alkali metal in the first portion is from about 0.2 nm to about 10 nm.

7. The TMD of any of 1 to 6, the TMD is selected from MoS<sub>2</sub>, WS<sub>2</sub>, MoSe<sub>2</sub> and WSe<sub>2</sub>, MoTe<sub>2</sub>, alkali metal-doped MoTe<sub>2</sub>, alkali metal-doped MoSe<sub>2</sub>, alkali metal-doped MoS<sub>2</sub>, alkali metal-doped WTe<sub>2</sub>, alkali metal-doped WSe<sub>2</sub>, or alkali metal-doped WS<sub>2</sub>.

15 8. An electronic device, including:

a layer of a transition metal dichalcogenide (TMD) including a first portion, wherein the first portion is surface modified with a Group 1 alkali metal; and  
a pair of electrodes connected to the layer of the TMD.

9. The electronic device of 8, having an electrical conductance of at least 4 times to that of a control.
10. The electronic device of 8 or 9, having a contact resistance of about  $1\text{ k}\Omega\text{ }\mu\text{m}$  to about  $10\text{ k}\Omega\text{ }\mu\text{m}$ .
- 5 11. The electronic device of any of 8 to 10, having an electron mobility of at least about  $70\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ .
12. The electronic device of any of 8 to 11, having a current on/off ratio of at least about 80.
13. The electronic device of any of 8 to 12, having a subthreshold swing (SS) of at least about  $60\text{ mV dec}^{-1}$ .
- 10 14. The electronic device of any of 8 to 13, having a voltage gain of about 100.
15. The electronic device of any of 8 to 14, having a power consumption of less than about  $10\text{ pW}$ .
16. The electronic device of any of 8 to 15, the electronic device is a logic inverter or a field effect transistor.
- 15 17. An electronic circuit comprising the electronic device of any of 8 to 16.
18. An electronic system comprising the electronic circuit of 17.