Claims

What is claimed is:

1. A semiconductor device, comprising:

a substrate comprising an active area;

a first gate line extending along a first direction on the active area;

a first gate line extension adjacent to the first gate line and outside the active area;

a second gate line extending along the first direction on the active area and adjacent to the first gate line; and

a second gate line extension adjacent to the second gate line and outside the active area,

wherein the first gate line extension and the second gate line extension are disposed at opposite outer sides of respective long sides of the first gate line and the second gate line.

2. The semiconductor device of claim 1, wherein the active area comprises a first indentation and a second indentation.

3. The semiconductor device of claim 2, wherein the first gate line extension overlaps the first indentation.

4. The semiconductor device of claim 2, wherein the second gate line extension overlaps the second indentation.

5. The semiconductor device of claim 1, further comprising:

a first doped region extending along a second direction between the first gate line and the second gate line; and

a second doped region around the first doped region and overlapping the active area.

6. The semiconductor device of claim 5, wherein the first doped region and the second doped region comprise different conductive type.

7. A semiconductor device, comprising:

a substrate comprising a first active area and a second active area;

a first gate line and a second gate line extending along a first direction on the first active area;

a third gate line and a fourth gate line extending along the first direction on the second active area;

a first gate line extension between the second gate line and the third gate line; and

a second gate line extension adjacent to the first gate line,

wherein the first gate line extension and the second gate line extension are disposed at opposite outer sides of respective long sides of the first gate line and the second gate line.

8. The semiconductor device of claim 7, wherein the first gate line extension connects the second gate line and the third gate line.

9. The semiconductor device of claim 7, further comprising:

a fifth gate line extending along the first direction adjacent to the first gate line;

a sixth gate line extending along the first direction adjacent to the fourth gate line;

the second gate line extension between the fifth gate line and the first gate line; and

a third gate line extension between the fourth gate line and the sixth gate line.

10. The semiconductor device of claim 9, wherein the second gate line extension connects the fifth gate line and the first gate line.

11. The semiconductor device of claim 9, wherein the third gate line extension connects the fourth gate line and the sixth gate line.

12. The semiconductor device of claim 9, wherein the active area comprises:

a first indentation between the second gate line and the third gate line;

a second indentation between the fifth gate line and the first gate line; and

a third indentation between the fourth gate line and the sixth gate line.

13. The semiconductor device of claim 12, wherein the first gate line extension overlaps the first indentation.

14. The semiconductor device of claim 12, wherein the second gate line extension overlaps the second indentation.

15. The semiconductor device of claim 12, wherein the third gate line extension overlaps the

third indentation.

16. The semiconductor device of claim 7, further comprising:

a first doped region extending along a second direction between the first gate line and the second gate line; and

a second doped region extending along the second direction between the third gate line and the fourth gate line.

17. The semiconductor device of claim 16, wherein the first doped region and the second doped region comprise same conductive type.