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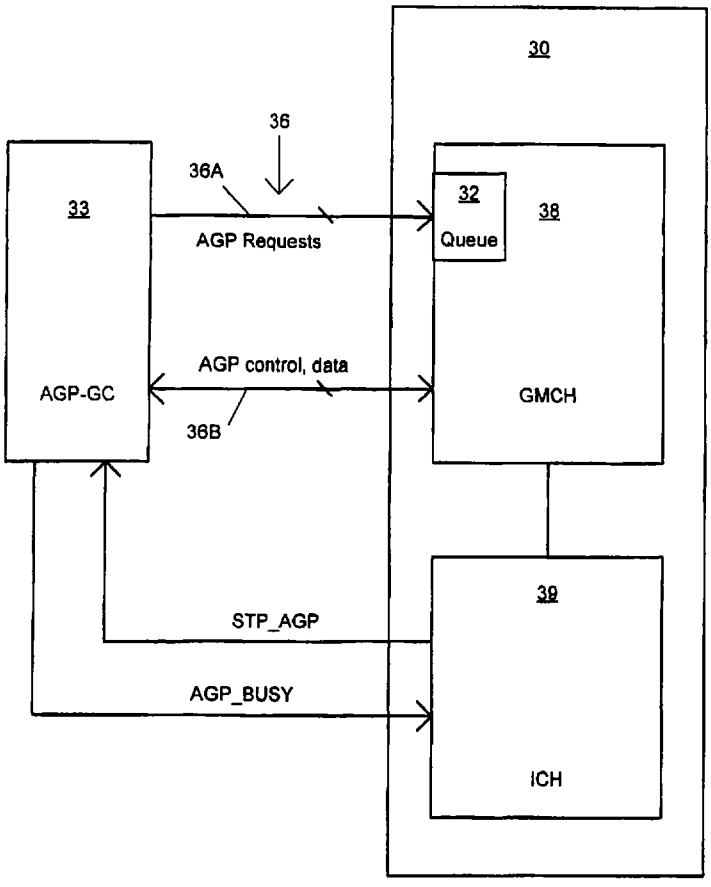
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(54) Title: ENTERING AND EXITING POWER MANAGED STATES WITHOUT DISRUPTING ACCELERATED GRAPHICS PORT TRANSACTIONS



(57) Abstract: An interface between an accelerated graphics port graphics controller (AGP-GC) and a core controller to prevent entry into a low power state from interfering with transfers to or from the AGP-GC that have been requested but not completed. The core controller can communicate to the AGP-GC an intent to enter a low power state, while the AGP-GC can communicate to the core controller the busy status of the AGP-GC. When the AGP-GC recieves notice of an intent to enter a low power state, it can stop issuing requests to the core controller. When the core controller detects that the AGP-GC is busy, the core controller can postpone entry into the low power state until the AGP-GC completes any requests that are in progress. In an alternate use of the interface, if the AGP-GC wishes to make a request during a low power state, it can signal the core controller of this need by indicating a busy status, which can trigger the core controller to initiate an exit from the low power state.

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