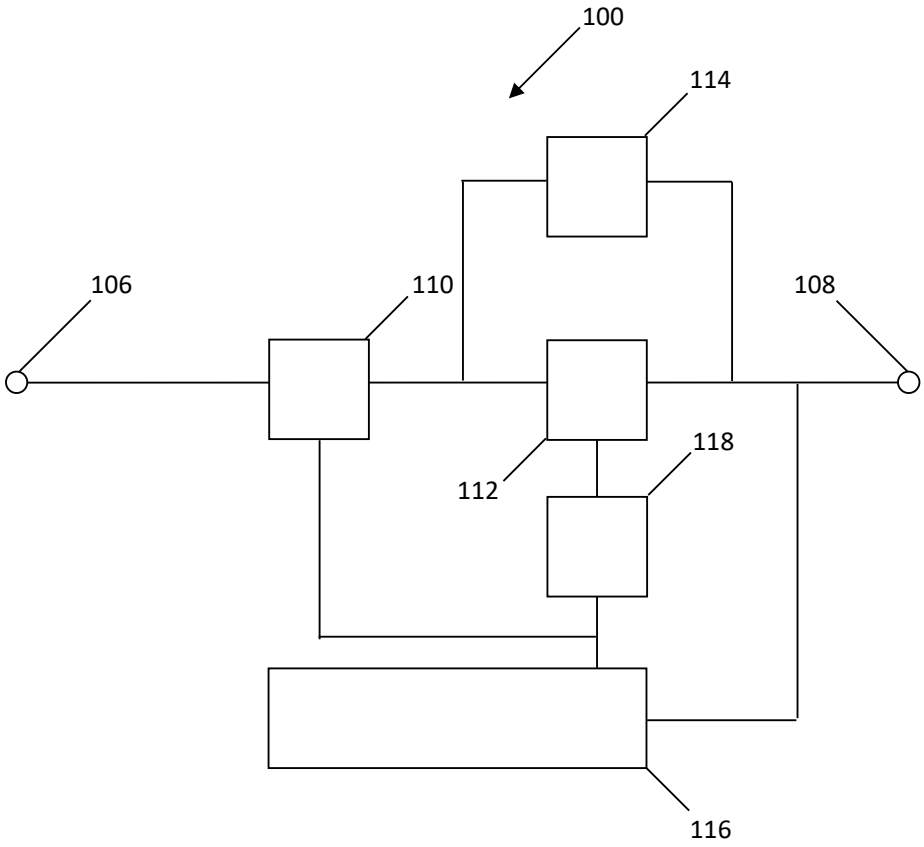


FIG. 1

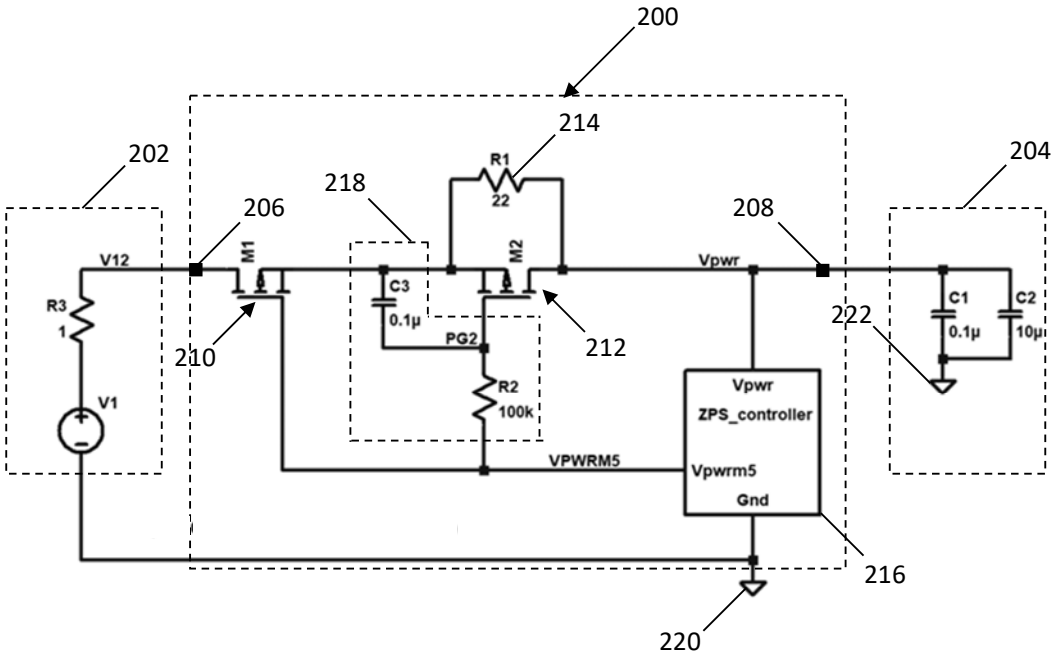

200
202
204
206
208
210
212
214
216
218
220
222
V12
R3
1
V1
M1
M2
C3
0.1µ
PG2
R1
22
R2
100k
Vpwr
VPWRM5
Vpwr
ZPS_controller
Vpwrm5
Gnd
C1
0.1µ
C2
10µ

FIG. 2

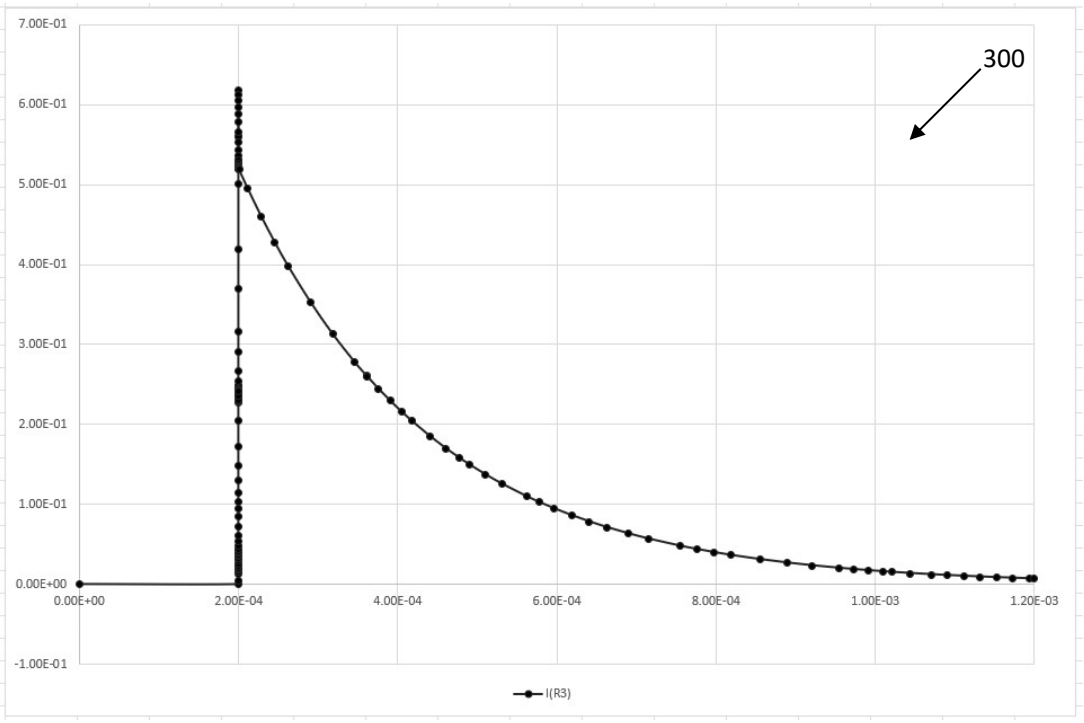

300
7.00E-01
6.00E-01
5.00E-01
4.00E-01
3.00E-01
2.00E-01
1.00E-01
0.00E+00
-1.00E-01
0.00E+00
2.00E-04
4.00E-04
6.00E-04
8.00E-04
1.00E-03
1.20E-03
I(R3)

FIG. 3A

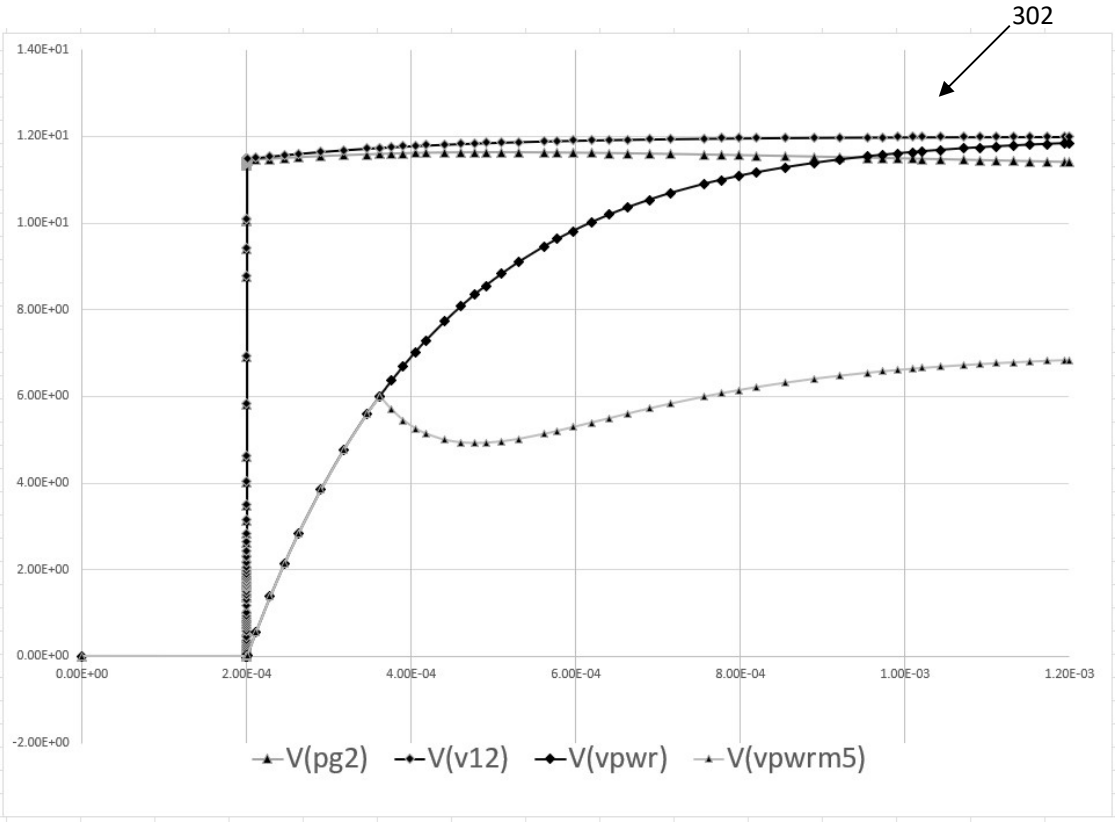

302
1.40E+01
1.20E+01
1.00E+01
8.00E+00
6.00E+00
4.00E+00
2.00E+00
0.00E+00
-2.00E+00
0.00E+00
2.00E-04
4.00E-04
6.00E-04
8.00E-04
1.00E-03
1.20E-03
V(pg2)
V(v12)
V(vpwr)
V(vpwrm5)

FIG. 3B

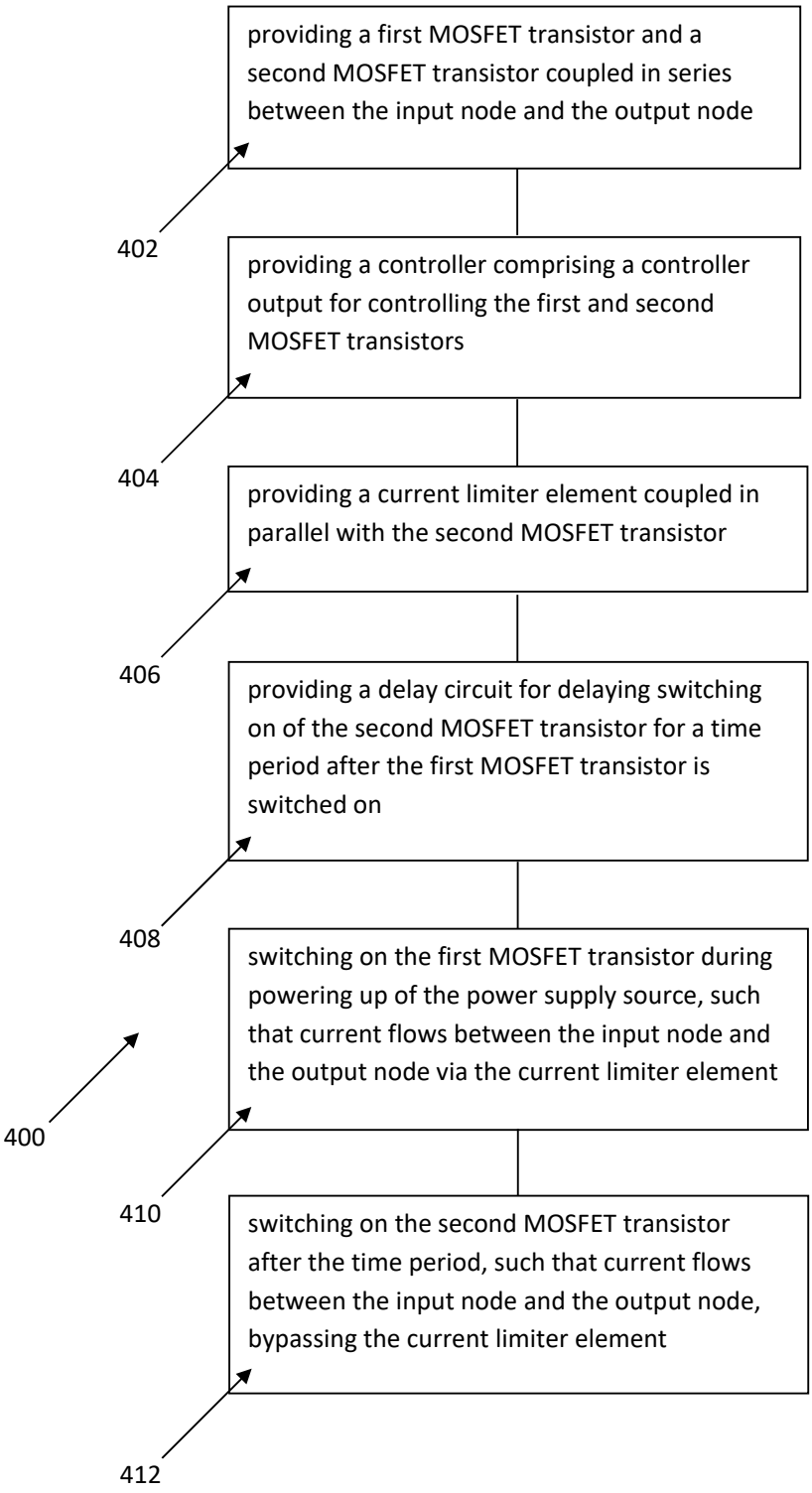

providing a first MOSFET transistor and a second MOSFET transistor coupled in series between the input node and the output node
402
providing a controller comprising a controller output for controlling the first and second MOSFET transistors
404
providing a current limiter element coupled in parallel with the second MOSFET transistor
406
providing a delay circuit for delaying switching on of the second MOSFET transistor for a time period after the first MOSFET transistor is switched on
408
switching on the first MOSFET transistor during powering up of the power supply source, such that current flows between the input node and the output node via the current limiter element
400
410
switching on the second MOSFET transistor after the time period, such that current flows between the input node and the output node, bypassing the current limiter element
412

FIG. 4