ABSTRACT

A FLASH ERASABLE SINGLE POLY EPROM DEVICE

A single polysilicon layer electrically programmable and electrically erasable read only memory cell is described. The cell utilizes an n-well inversion capacitor, formed in a semiconductor substrate as the control gate. One plate of the capacitor is formed from the same polysilicon layer as the floating gate of the memory device, thus capacitively coupling the floating gate and the inversion capacitor control gate. Additional erase performance is achieved by addition of a dedicated erase capacitor to the basic cell. Still further improvement in programming performance and protection against over-erase failure in a flash type EEPROM device is achieved by the addition of a select transistor. Prevention of program disturb and DC erase is also described.

(Fig. 1)

