CLAIMS

What is claimed is:

1. An apparatus, comprising:

a die including a through-silicon via and a radio frequency integrated circuit (TSV RFIC die); and

a phased-array antenna (PAA) substrate vertically integrated with the TSV RFIC, wherein the PAA substrate includes a plurality of antenna elements, each of which is coupled to the TSV RFIC through a plurality of TSVs.

2. The apparatus of claim 1, further including a first-level interconnect substrate onto which the TSV RFIC is mounted.

3. The apparatus of claim 1, further including a first-level interconnect substrate onto which the TSV RFIC is mounted, and wherein the first-level interconnect substrate includes at least one passive device embedded therein that functions with the TSV RFIC.

4. The apparatus of claim 1, further including:

a first-level interconnect substrate onto which the TSV RFIC is mounted, wherein the TSV RFIC includes an active surface and a backside surface;

a plurality of plurality of electrical bumps disposed between the active surface and the first-level interconnect substrate, wherein the first-level interconnect substrate is a secondary package substrate; and

a plurality of backside bumps disposed between the backside surface and the PAA substrate.

5. The apparatus of claim 1, wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through inductive-coupling apertures in the PAA substrate.

6. The apparatus of claim 1, wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through via-coupling in the PAA substrate.

7. The apparatus of claim 1, wherein the PAA substrate includes a first dielectric layer and

a second dielectric layer, wherein the first dielectric layer is closer to the plurality of antenna elements and the second dielectric layer is closer to the TSV RFIC, and where the first dielectric layer has a lower dielectric constant than the second dielectric layer.

8. The apparatus of claim 1, wherein the PAA substrate includes a first dielectric layer and a second dielectric layer, wherein the first dielectric layer is glass and is closer to the plurality of antenna elements and the second dielectric layer is glass and is closer to the TSV RFIC, and where the first dielectric layer has a lower dielectric constant than the second dielectric layer.

9. The apparatus of claim 1, wherein the PAA substrate includes an embedded ground plane coupled to the plurality of antenna elements and also coupled to the TSV RFIC.

10. The apparatus of claim 1, further including:

a first-level interconnect substrate onto which the TSV RFIC is mounted, wherein the PAA substrate includes an embedded ground plane coupled to the plurality of antenna elements and also coupled to the TSV RFIC; and

at least one dummy bump disposed between the PAA substrate and the substrate onto which the TSV RFIC is mounted.

11. The apparatus of claim 1, wherein the TSV RFIC is embedded in a bumpless, build-up layer (BBUL) that is coupled to the PAA substrate.

12. The apparatus of claim 1, wherein the TSV RFIC is embedded in a BBUL that is coupled to the PAA substrate, and wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through inductive-coupling apertures in the PAA substrate.

13. The apparatus of claim 1, wherein the TSV RFIC is embedded in a BBUL that is coupled to the PAA substrate, and wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through via-coupling in the PAA substrate.

14. The apparatus of claim 1, wherein the TSV RFIC is embedded in a BBUL that is coupled to the PAA substrate, further including a first-level interconnect substrate onto which the TSV RFIC is mounted, and wherein the first-level interconnect substrate includes at least

one passive device embedded therein that functions with the TSV RFIC.

15. The apparatus of claim 1, further including a through-silicon via digital processor die (TSV DP) coupled to the TSV RFIC through at least one TSV in the TSV RFIC and at least one TSV in the TSV DP, and wherein the TSV DP and the TSV RFIC are vertically integrated below the PAA substrate.

16. The apparatus of claim 1, further including a through-silicon via digital processor die (TSV DP) coupled to the TSV RFIC through at least one TSV in the TSV RFIC and at least one TSV in the TSV DP, and wherein the TSV DP and the TSV RFIC are vertically integrated below the PAA substrate, wherein the PAA substrate includes an embedded ground plane coupled to the plurality of antenna elements and also coupled to the TSV RFIC.

17. The apparatus of claim 1, further including:

a through-silicon via digital processor die (TSV DP) coupled to the TSV RFIC through at least one TSV in the TSV RFIC and at least one TSV in the TSV DP, and wherein the TSV DP and the TSV RFIC are vertically integrated below the PAA substrate;

a first-level interconnect substrate onto which the TSV DP is mounted, wherein the PAA substrate includes an embedded ground plane coupled to the plurality of antenna elements and also coupled to the TSV RFIC; and

at least one dummy bump disposed between the PAA substrate and the substrate onto which the TSV RFIC is mounted.

18. The apparatus of claim 1, further including:

a through-silicon via digital processor die (TSV DP) coupled to the TSV RFIC through at least one TSV in the TSV RFIC and at least one TSV in the TSV DP, and wherein the TSV DP and the TSV RFIC are vertically integrated below the PAA substrate; and.

a first-level interconnect substrate onto which the TSV DP is mounted, and wherein the first-level interconnect substrate includes at least one passive device embedded therein that functions with the TSV RFIC.

19. An apparatus, comprising:

a die including a through-silicon via and a radio frequency integrated circuit (TSV RFIC die) including an active surface and a backside surface; and

a phased-array antenna (PAA) substrate vertically integrated with the TSV RFIC, wherein the PAA substrate includes a plurality of antenna elements, each of which is coupled to the TSV RFIC through electrical bumps on the active surface.

20. The apparatus of claim 19, further including a first-level interconnect substrate onto which the TSV RFIC is mounted, wherein the TSV RFIC is contacted to the first-level interconnect substrate through TSVs in the TSV RFIC die.

21. A process of forming a vertically integrated apparatus comprising:

assembling a through-silicon via radio-frequency integrated circuit die (TSV RFIC) to a phased-array antenna (PAA) substrate, wherein the PAA substrate includes a plurality of antenna elements, and wherein assembling includes coupling each antenna element to a TSV in the TSV RFIC.

22. The process of claim 21, wherein the TSV RFIC includes an active surface and a backside surface, further including:

testing the apparatus, followed by;

assembling the apparatus to a first-level interconnect board by coupling each the active surface to a plurality of electrical bumps between the TSV RFIC and the first-level interconnect.

23. The process of claim 21, wherein the TSV RFIC includes an active surface and a backside surface, further including:

assembling the apparatus to a first-level interconnect board by coupling each the active surface to a plurality of electrical bumps between the TSV RFIC and the first-level interconnect, followed by;

testing the apparatus.

24. The process of claim 21, wherein the TSV RFIC includes an active surface and a backside surface, the process further including assembling the apparatus to a first-level interconnect substrate by coupling each the active surface to a plurality of electrical bumps between the TSV RFIC and the first-level interconnect.

25. The process of claim 21, wherein before assembling the TSV RFIC to the PAA

substrate, the TSV is first embedded in a bumpless, build-up layer (BBUL).

26. The process of claim 21, further including assembling a through-silicon via digital processor to the TSV RFIC die.

27. The process of claim 21, further including assembling the apparatus to a computing system.

28. The process of claim 21, further including operating a remote device through the apparatus.

29. A computer system comprising:

a die including a through-silicon via and a radio frequency integrated circuit (TSV RFIC die);

a phased-array antenna (PAA) substrate vertically integrated with the TSV RFIC, wherein the PAA substrate includes a plurality of antenna elements, each of which is coupled to the TSV RFIC through a plurality of TSVs;

a first-level interconnect substrate onto which the TSV RFIC is mounted; and

a foundation substrate that supports the first-level interconnect substrate.

30. The computer system of claim 29, wherein the foundation substrate is part of a mobile device.

31. The computer system of claim 29, wherein the foundation substrate is part of a vehicle.

32. The computer system of claim 29, wherein the foundation substrate is part of a television.

CLAIMS
What is claimed is:

1. An apparatus, comprising:
a die including a through-silicon via and a radio frequency integrated circuit (TSV RFIC die);

a phased-array antenna (PAA) substrate vertically integrated with the TSV RFIC, wherein the PAA substrate includes a plurality of antenna elements, each of which is coupled to the TSV RFIC through a plurality of TSVs;

a first-level interconnect substrate onto which the TSV RFIC is mounted, wherein the TSV RFIC includes an active surface and a backside surface;

a plurality of plurality of electrical bumps disposed between the active surface and the first-level interconnect substrate, wherein the first-level interconnect substrate is a secondary package substrate; and

a plurality of backside bumps disposed between the backside surface and the PAA substrate.

2. The apparatus of claim 1, wherein the first-level interconnect substrate includes at least one passive device embedded therein that functions with the TSV RFIC.

3. The apparatus of claim 1, wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through inductive-coupling apertures in the PAA substrate.

4. The apparatus of claim 1, wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through via-coupling in the PAA substrate.

5. The apparatus of claim 1, wherein the PAA substrate includes a first dielectric layer and a second dielectric layer, wherein the first dielectric layer is closer to the plurality of antenna elements and the second dielectric layer is closer to the TSV RFIC, and where the first dielectric layer has a lower dielectric constant than the second dielectric layer.

6. The apparatus of claim 1, wherein the PAA substrate includes a first dielectric layer and a second dielectric layer, wherein the first dielectric layer is glass and is closer to the plurality of antenna elements and the second dielectric layer is glass and is closer to the TSV RFIC, and where the first dielectric layer has a lower dielectric constant than the second dielectric layer.

7. The apparatus of claim 1, wherein the PAA substrate includes an embedded ground plane coupled to the plurality of antenna elements and also coupled to the TSV RFIC.

8. The apparatus of claim 7, further including:
at least one dummy bump disposed between the PAA substrate and the substrate onto which the TSV RFIC is mounted.

9. The apparatus of claim 1, wherein the TSV RFIC is embedded in a bumpless, build-up layer (BBUL) that is coupled to the PAA substrate.

10. The apparatus of claim 1, wherein the TSV RFIC is embedded in a BBUL that is coupled to the PAA substrate, and wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through inductive-coupling apertures in the PAA substrate.

11. The apparatus of claim 1, wherein the TSV RFIC is embedded in a BBUL that is coupled to the PAA substrate, and wherein the plurality of antenna elements in the PAA substrate is coupled to the TSV RFIC through via-coupling in the PAA substrate.

12. The apparatus of claim 1, wherein the TSV RFIC is embedded in a BBUL that is coupled to the PAA substrate, further including a first-level interconnect substrate onto which the TSV RFIC is mounted, and wherein the first-level interconnect substrate includes at least one passive device embedded therein that functions with the TSV RFIC.

13. The apparatus of claim 1, further including a through-silicon via digital processor die (TSV DP) coupled to the TSV RFIC through at least one TSV in the TSV RFIC and at least one TSV in the TSV DP, and wherein the TSV DP and the TSV RFIC are vertically integrated below the PAA substrate.

14. The apparatus of claim 1, further including a through-silicon via digital processor die (TSV DP) coupled to the TSV RFIC through at least one TSV in the TSV RFIC and at least one TSV in the TSV DP, and wherein the TSV DP and the TSV RFIC are vertically integrated below the PAA substrate, wherein the PAA substrate includes an embedded ground plane coupled to the plurality of antenna elements and also coupled to the TSV RFIC.

15. An apparatus, comprising:
a die including a through-silicon via and a radio frequency integrated circuit (TSV RFIC die);

a phased-array antenna (PAA) substrate vertically integrated with the TSV RFIC, wherein the PAA substrate includes a plurality of antenna elements, each of which is coupled to the TSV RFIC through a plurality of TSVs;

a through-silicon via digital processor die (TSV DP) coupled to the TSV RFIC through at least one TSV in the TSV RFIC and at least one TSV in the TSV DP, and wherein the TSV DP and the TSV RFIC are vertically integrated below the PAA substrate;

a first-level interconnect substrate onto which the TSV DP is mounted, wherein the PAA substrate includes an embedded ground plane coupled to the plurality of antenna elements and also coupled to the TSV RFIC; and

at least one dummy bump disposed between the PAA substrate and the substrate onto which the TSV RFIC is mounted.

16. The apparatus of claim 15, wherein the first-level interconnect substrate includes at least one passive device embedded therein that functions with the TSV RFIC.

17. A process of forming a vertically integrated apparatus comprising:

assembling a through-silicon via radio-frequency integrated circuit die (TSV RFIC) to a phased-array antenna (PAA) substrate, wherein the PAA substrate includes a plurality of antenna elements, and wherein assembling includes coupling each antenna element to a TSV in the TSV RFIC;

mounting the TSV RFIC to a first-level interconnect substrate, wherein the TSV RFIC includes an active surface and a backside surface by disposing a plurality of plurality of electrical bumps between the active surface and the first-level interconnect substrate, wherein the first-level interconnect substrate is a secondary package substrate; and

disposing a plurality of backside bumps between the backside surface and the PAA substrate.

18. The process of claim 17, further including:
testing the apparatus, followed by;

mounting the TSV RFIC to the first-level interconnect.

19. The process of claim 17, further including:
testing the apparatus, after mounting the TSV RFIC to the first-level interconnect.

20. The process of claim 17, wherein before assembling the TSV RFIC to the PAA substrate, the TSV is first embedded in a bumpless, build-up layer (BBUL).

21. The process of claim 17, further including assembling a through-silicon via digital processor to the TSV RFIC die.

22. The process of claim 17, further including assembling the apparatus to a computing system.

23. The process of claim 17, further including operating a remote device through the apparatus.

24. A computer system comprising:
a die including a through-silicon via and a radio frequency integrated circuit (TSV RFIC die);

a phased-array antenna (PAA) substrate vertically integrated with the TSV RFIC, wherein the PAA substrate includes a plurality of antenna elements, each of which is coupled to the TSV RFIC through a plurality of TSVs;

a first-level interconnect substrate onto which the TSV RFIC is mounted, wherein the TSV RFIC includes an active surface and a backside surface;

a plurality of plurality of electrical bumps disposed between the active surface and the first-level interconnect substrate, wherein the first-level interconnect substrate is a secondary package substrate;

a plurality of backside bumps disposed between the backside surface and the PAA substrate; and

a foundation substrate that supports the first-level interconnect substrate.

25. The computer system of claim 24, wherein the foundation substrate is part of a mobile device.

26. The computer system of claim 24, wherein the foundation substrate is part of a vehicle.

27. The computer system of claim 24, wherein the foundation substrate is part of a television.