

## **HIGH VOLTAGE DEVICE**

### **ABSTRACT**

A device is disclosed. The device includes a substrate prepared with an active device region. The active device region includes a gate. The device also includes a doped channel well disposed in the substrate adjacent to a first edge of the gate. The first edge of the gate overlaps the channel well with a channel edge of the channel well beneath the gate. The first edge of the gate and channel edge defines an effective channel length of the device. The effective channel length is self-aligned to the gate. A doped drift well adjacent to a second edge of the gate is also included.

Fig. 1