processor; a digital scaling unit coupled to outputs of the ADC unit; and a digital accumulator coupled to outputs of the digital scaling unit, wherein the digital accumulator comprises a memory unit and a digital adder.

[0044] In some embodiments, the hybrid analog-digital processor further comprises an amplification or attenuation unit coupled between the DAC unit and the ADC unit.

[0045] In some embodiments, the analog processor comprises a photonic processor comprising a plurality of programmable photonic devices.

[0046] In some embodiments, the programmable photonic devices comprise Mach-Zehnder interferometers.

[0047] In some embodiments, the programmable photonic devices comprise optical resonators.

[0048] In some embodiments, the analog processor is programmed with a plurality of matrices that, collectively, represent an arbitrary matrix.

[0049] In some embodiments, the plurality of matrices collectively represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

[0050] In some embodiments, the plurality of matrices collectively represent the arbitrary matrix based on a dilation of the arbitrary matrix.

[0051] According to a first aspect of the present invention, there is provided a hybrid analog-digital processor configured to perform a matrix multiplication, comprising: circuitry comprising an optical analog processor and an optical analog scaling unit, wherein the circuitry is configured to: generate a plurality of optical input analog signals based on an input data set, the plurality of optical input analog signals representing a matrix to be multiplied in the matrix multiplication; set a gain of the optical analog scaling unit based on a scaling factor; program the optical analog processor with a set of parameters representing a further matrix to be multiplied in the matrix multiplication; generate a plurality of optical output analog signals based on the plurality of input analog signals and the set of parameters, the plurality of optical output analog signals representing the multiplication between the matrix and the further matrix; generate a plurality of amplified or attenuated optical output analog signals by amplifying or attenuating, using the optical analog scaling unit, the plurality of optical input analog signals and/or the plurality of optical output analog signals; and generate an output data set based on the plurality of amplified or attenuated optical output analog signals.

[0052] In some embodiments, the analog scaling unit comprises an analog amplifier or attenuator.

[0053] In some embodiments, the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to: set the gain of the analog scaling unit to a first value during a first pass of the multi-pass computation; and set the gain of the analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

[0054] In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

[0055] In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

[0056] In some embodiments, the circuitry comprises a plurality of analog-to-digital converters (ADCs), and the plurality of ADCs are configured to generate the output data set based on the plurality of output analog signals.

[0057] In some embodiments, the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

[0058] In some embodiments, programming the analog processor comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

[0059] In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

[0060] In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

[0061] In some embodiments, the circuitry is further configured to determine the scaling factor based on the set of parameters and the input data set.

[0062] In some embodiments, determining the scaling factor comprises determining the scaling factor based on statistics bounds on the set of parameters and statistical bounds on the input data set.

[0063] According to a second aspect of the present invention, there is provided a method for performing a matrix multiplication, the method comprising: generating a plurality of optical input analog signals based on an input data set, the plurality of optical input analog signals representing a matrix to be multiplied in the matrix multiplication; setting a gain of an optical analog scaling unit based on one or more scaling factors; programming an optical analog processor with a set of parameters representing a further matrix to be multiplied in the matrix multiplication; generating a plurality of optical output analog signals based on the

plurality of optical input analog signals and the set of parameters, the plurality of optical analog signals representing the multiplication between the matrix and the further matrix; generating a plurality of amplified or attenuated optical output analog signals by amplifying or attenuating, using the optical analog scaling unit, the

plurality of optical input analog signals and/or the plurality of optical output analog signals; and generating an output data set based on the plurality of amplified or attenuated optical output analog signals.

[0064] In some embodiments, the analog scaling unit comprises an analog amplifier or attenuator.

[0065] In some embodiments, the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to: set the gain of the analog scaling unit to a first value during a first pass of the multi-pass computation; and set the gain of the analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

[0066] In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

[0067] In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

[0068] In some embodiments, the circuitry comprises a plurality of analog-to-digital converters (ADCs), and the plurality of ADCs are configured to generate the output data set based on the plurality of output analog signals.

[0069] In some embodiments, the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

[0070] In some embodiments, programming the analog processor comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

[0071] In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

[0072] In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

[0073] In some embodiments, the method further comprises determining the scaling factor based on the set of parameters and the input data set.

[0089] In some embodiments, the photonic processor comprises a plurality of optical resonators.

[0090] In some embodiments, the photonic processor comprises a first array of interconnected variable beam splitters (VBSs) comprising a first plurality of optical inputs and a first plurality of optical outputs; a second array of interconnected VBSs comprising a second plurality of optical inputs and a second plurality of optical outputs; and a plurality of controllable optical elements, each of the plurality of these controllable optical elements coupling a single one of the first plurality of optical outputs of the first array to a respective single one of the second plurality of optical inputs of the second array.

[0091] In some embodiments, the photonic processor is programmed with a plurality of matrices that, collectively, represent an arbitrary matrix.

[0092] According to a third aspect of the present invention, there is provided a hybrid analog-digital processor configured to perform a matrix multiplication, comprising circuitry comprising a photonic processor and at least one amplifier, wherein the circuitry is configured to: generate a plurality of optical input analog signals based on an input data set, the plurality of optical input analog signals representing a matrix to be multiplied in the matrix multiplication; set a gain of the at least one amplifier based on one or more scaling factors; program the photonic processor with a set of parameters representing a further matrix to be multiplied in the matrix multiplication; generate a plurality of optical output analog signals based on the plurality of optical input analog signals and the set of parameters; generate a plurality of output analog signals based on the plurality of optical output analog signals; generate a plurality of amplified output signals by amplifying, using the at least one amplifier, at least one among the plurality of optical input analog signals, the plurality of optical output analog signals and the plurality of output analog signals; and generate an output data set based on the plurality of amplified output signals.

[0093] In some embodiments, the at least one amplifier comprises an optical amplifier and an electronic amplifier, wherein amplifying, using the at least one amplifier, at least one among the plurality of input optical signals, the plurality of output optical signals and the plurality of output analog signals comprises: amplifying the plurality of input optical signals with the optical amplifier; and amplifying the plurality of output analog signals with the electronic amplifier.

[0094] In some embodiments, the at least one amplifier comprises a laser, and wherein setting the gain of the amplifier comprises setting a gain of the laser.

[0095] In some embodiments, the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to: set the gain of the at least one amplifier to a first value during a first pass

CLAIMS

What is claimed is:

1. A hybrid analog-digital processor configured to perform a matrix multiplication, comprising:

circuitry comprising an optical analog processor and an optical analog scaling unit, wherein the circuitry is configured to:

generate a plurality of optical input analog signals based on an input data set, the plurality of optical input analog signals representing a matrix to be multiplied in the matrix multiplication;

set a gain of the optical analog scaling unit based on one or more scaling factors;

program the optical analog processor with a set of parameters representing a further matrix to be multiplied in the matrix multiplication;

generate a plurality of optical output analog signals based on the plurality of optical input analog signals and the set of parameters, the plurality of optical output analog signals representing the multiplication between the matrix and the further matrix;

generate a plurality of amplified or attenuated optical output analog signals by amplifying or attenuating, using the optical analog scaling unit, the plurality of optical input analog signals and/or the plurality of optical output analog signals; and

generate an output data set based on the plurality of amplified or attenuated optical output analog signals.

2. The hybrid analog-digital processor of claim 1, wherein the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the matrix multiplication, wherein the circuitry is further configured to:

set the gain of the optical analog scaling unit to a first value during a first pass of the multi-pass computation; and

set the gain of the optical analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

3. The hybrid analog-digital processor of claim 1, wherein the circuitry comprises a plurality of analog-to-digital converters (ADCs), and the plurality of ADCs are configured to

generate the output data set based on the plurality of optical output analog signals, wherein the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

4. The hybrid analog-digital processor of claim 1, wherein programming the optical analog processor comprises:

programming, based on the set of parameters, the optical analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

5. The hybrid analog-digital processor of claim 4, wherein programming the optical analog processor with a plurality of matrices comprises:

programming, based on the set of parameters, the optical analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

6. The hybrid analog-digital processor of claim 1, wherein the circuitry is further configured to determine the one or more scaling factors based on the set of parameters and the input data set.

7. The hybrid analog-digital processor of claim 1, wherein determining the one or more scaling factors comprises determining the one or more scaling factors based on statistical bounds on the set of parameters and statistical bounds on the input data set.

8. A method for performing a matrix multiplication, the method comprising:

generating a plurality of optical input analog signals based on an input data set, the plurality of optical input analog signals representing a matrix to be multiplied in the matrix multiplication;

setting a gain of an optical analog scaling unit based on one or more scaling factors;

programming an optical analog processor with a set of parameters representing a further matrix to be multiplied in the matrix multiplication;

generating a plurality of optical output analog signals based on the plurality of optical input analog signals and the set of parameters, the plurality of optical output analog signals representing the multiplication between the matrix and the further matrix;

generating a plurality of amplified or attenuated optical output analog signals by amplifying or attenuating, using the optical analog scaling unit, the plurality of optical input analog signals and/or the plurality of optical output analog signals; and

generating an output data set based on the plurality of amplified or attenuated optical output analog signals.

9. The method of claim 8, wherein the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the matrix multiplication, wherein the circuitry is further configured to:

set the gain of the analog scaling unit to a first value during a first pass of the multi-pass computation; and

set the gain of the analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

10. The method of claim 8, wherein programming the optical analog processor comprises:

programming, based on the set of parameters, the optical analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

11. The method of claim 10, wherein programming the optical analog processor with a plurality of matrices comprises:

programming, based on the set of parameters, the optical analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

12. The method of claim 8, further comprising determining the one or more scaling factors based on the set of parameters and the input data set.

13. The method of claim 12, wherein determining the one or more scaling factors comprises determining the one or more scaling factors based on statistical bounds on the set of parameters and statistical bounds on the input data set.

14. A hybrid analog-digital processor configured to perform a matrix multiplication, comprising:

circuitry comprising a photonic processor and at least one amplifier, wherein the circuitry is configured to:

generate a plurality of optical input analog signals based on an input data set, the plurality of optical input analog signals representing a matrix to be multiplied in the matrix multiplication;

set a gain of the at least one amplifier based on one or more scaling factors;

program the photonic processor with a set of parameters representing a further matrix to be multiplied in the matrix multiplication;

generate a plurality of optical output analog signals based on the plurality of optical input analog signals and the set of parameters;

generate a plurality of output analog signals based on the plurality of optical output analog signals;

generate a plurality of amplified output signals by amplifying, using the at least one amplifier, at least one among the plurality of optical input analog signals, the plurality of optical output analog signals and the plurality of output analog signals; and

generate an output data set based on the plurality of amplified output signals.

15. The hybrid analog-digital processor of claim 14, wherein the at least one amplifier comprises an optical amplifier and an electronic amplifier, wherein amplifying, using the at least one amplifier, at least one among the plurality of input optical signals, the plurality of optical output analog signals and the plurality of output analog signals comprises:

amplifying the plurality of optical input analog signals with the optical amplifier; and

amplifying the plurality of output analog signals with the electronic amplifier.

16. The hybrid analog-digital processor of claim 14, wherein the at least one amplifier comprises a laser, and wherein setting the gain of the amplifier comprises setting a gain of the laser.

17. The hybrid analog-digital processor of claim 14, wherein the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the matrix multiplication, wherein the circuitry is further configured to:

set the gain of the at least one amplifier to a first value during a first pass of the multi-pass computation; and

set the gain of the at least one amplifier to a second value, different from the first value, during a second pass of the multi-pass computation.

20. The hybrid analog-digital processor of claim 14, wherein the photonic processor comprises a plurality of optical resonators.

21. The hybrid analog-digital processor of claim 14, wherein the photonic processor comprises:

a first array of interconnected variable beam splitters (VBSs) comprising a first plurality of optical inputs and a first plurality of optical outputs;

a second array of interconnected VBSs comprising a second plurality of optical inputs and a second plurality of optical outputs; and

a plurality of controllable optical elements, each of the plurality of these controllable optical elements coupling a single one of the first plurality of optical outputs of the first array to a respective single one of the second plurality of optical inputs of the second array.

22. The hybrid analog-digital processor of claim 14, wherein programming the photonic processor comprises:

programming, based on the set of parameters, the photonic processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

23. The hybrid analog-digital processor of claim 22, wherein programming the photonic processor with a plurality of matrices comprises:

programming, based on the set of parameters, the photonic processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

24. The hybrid analog-digital processor of claim 22, wherein programming the photonic processor with a plurality of matrices comprises:

programming, based on the scaled set of parameters, the photonic processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

25. The hybrid analog-digital processor of claim 14, wherein the circuitry is further configured to determine the one or more scaling factors based on the set of parameters and the input data set.

26. The hybrid analog-digital processor of claim 25, wherein determining the one or more scaling factors comprises determining the one or more scaling factors based on statistical bounds on the set of parameters and statistical bounds on the input data set.