According to the present invention, there can be provided a method for producing an SGT in which a thin gate material is used, a metal gate is employed, and a self-aligned process is performed and an SGT structure obtained by the method.

The height of each of the first pillar-shaped silicon layer ~~104~~ and second pillar-shaped silicon layer ~~105~~ is set to be the sum of a desired height of the pillar-shaped silicon layer and the height of a portion removed by gate-line etching performed later, whereby a self-aligned process is achieved.

[0021]

The method for producing an SGT includes:

a second step including forming a gate insulating film around each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer,

forming a metal film and a polysilicon film around the gate insulating film,

the thickness of the polysilicon film being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer,

forming a third resist for forming a gate line, and

forming the gate line by performing anisotropic etching; and

a third step including, after the second step,

depositing a fourth resist so that a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer is exposed, removing the exposed portion of the polysilicon film by etching, removing the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode connected to the gate line.

Therefore, a self-aligned process is achieved.

Such a self-aligned process allows high degree of integration.

[0022]

The gate line has a laminated structure of the metal film and a silicide. A direct contact between the silicide and the metal film can decrease the resistance.

[0023]

The thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the metal film and polysilicon film.

Even when a ~~seventh~~ resist for forming contact holes is formed in a misaligned manner and contact holes are formed by overetching, a short circuit between a contact and the gate electrode can be prevented.

[0024]

Furthermore, the third resist 112 is preferably formed so that the center line of the third resist 112 for forming the gate line is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105. This is because a silicide that connects a second n-type diffusion layer 118 to a second p-type diffusion layer 121 is easily formed.

[0039]

Next, as shown in Fig. 11, the polysilicon film 111 and the metal film 110 are etched.

As a result, a polysilicon film 111a, a polysilicon film 111b, and a polysilicon film wiring 111c are formed. Herein, if the thickness of the resist on the upper portion of each of the pillar-shaped silicon layers is small or the polysilicon film on the upper portion of each of the pillar-shaped silicon layers is exposed, the upper portion of each of the pillar-shaped silicon layers may be etched during the etching. In such a case, when each of the pillar-shaped silicon layers is formed, the height of the pillar-shaped silicon layer may be set to be the sum of a desired height of the pillar-shaped silicon layer and the height of a portion removed by gate-line etching performed later. Therefore, the production process of the present invention is a self-aligned process.

portions of the polysilicon films 111a and 111b by etching, removing the fourth resist 113, and removing the metal film 110 by etching to form a first gate electrode 114b and a second gate electrode 114a connected to the gate line 114c.

[0042]

As shown in Fig. 13, a fourth resist 113 is deposited so that portions of the polysilicon films 111b and 111a on upper side walls of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 are exposed. This is preferably performed by resist etch back. A coating film such as a spin-on-glass film may also be used.

[0043]

Next, as shown in Fig. 14, the exposed portions of the polysilicon films 111a and 111b are removed by etching. This is preferably performed by isotropic dry etching.

[0044]

Next, as shown in Fig. 15, the fourth resist 113 is removed.

[0045]

Next, as shown in Fig. 16, the metal film 110 is removed by etching to form a metal film 110b on a side wall of the first pillar-shaped silicon layer 104, a metal film 110a on a side wall of the second pillar-shaped silicon layer 105, and a metal film 110c below the polysilicon film wiring 111c. This is preferably performed by isotropic etching.

The metal film 110b and the polysilicon film 111b constitute a first gate electrode 114b.

The metal film 110a and the polysilicon film 111a constitute a second gate electrode 114a.

The metal film 110c and the polysilicon film wiring 111c constitute a gate line 114c. Therefore, this process is a self-aligned process.

[0046]

The third step has been described, the third step including depositing a fourth resist 113 so that portions of the polysilicon films 111b and 111a on upper side walls of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 are exposed, removing the exposed portions of the polysilicon films 111a and 111b by etching, removing the fourth resist 113, and removing the metal film 110 by etching to form a first gate electrode 114b and a second gate electrode 114a connected to the gate line 114c.

[0047]

A fourth step will now be described. The fourth step includes forming a first n-type diffusion layer 117 in an upper portion of the first pillar-shaped silicon layer 104,

forming a second n-type diffusion layer 118 in a lower portion of the first pillar-shaped silicon layer 104 and in an upper portion of the planar silicon layer 107,

forming a first p-type diffusion layer 120 in an upper

CLAIMS

[Claim 1]

A method for producing a semiconductor device, the method comprising:

a first step including forming a planar silicon layer on a silicon substrate, and

forming a first pillar-shaped silicon layer and a second pillar-shaped silicon layer on the planar silicon layer;

a second step including, after the first step, forming a gate insulating film around each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer,

forming a metal film and a polysilicon film around the gate insulating film,

the thickness of the polysilicon film being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer,

forming a third resist for forming a gate line, and

forming the gate line by performing anisotropic etching; and

a third step including, after the second step, depositing a fourth resist so that a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer is exposed, removing the exposed portion of the

polysilicon film by etching, removing the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode connected to the gate line.

[Claim 2]

The method for producing a semiconductor device according to Claim 1, wherein upper portions of the first pillar-shaped silicon layer and second pillar-shaped silicon layer are etched by the anisotropic etching.

[Claim 3]

The method for producing a semiconductor device according to Claim 1, wherein an upper surface of the third resist for forming the gate line is located at a lower position than an upper surface of the polysilicon film on each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer.

[Claim 4]

The method for producing a semiconductor device according to Claim 1, further comprising a fourth step including forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer,

forming a second n-type diffusion layer in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer,

forming a first p-type diffusion layer in an upper

portion of the second pillar-shaped silicon layer, and

forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[Claim 5]

The method for producing a semiconductor device according to Claim 4, further comprising a fifth step including forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

[Claim 6]

A semiconductor device comprising:

a planar silicon layer formed on a silicon substrate;

first and second pillar-shaped silicon layers formed on the planar silicon layer;

a gate insulating film formed around the first pillar-shaped silicon layer;

a first gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

a gate insulating film formed around the second pillar-shaped silicon layer;

a second gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are

formed around the gate insulating film;

the thickness of each of the polysilicon films being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer;

a gate line connected to the first and second gate electrodes;

an upper surface of the gate line being located at a lower position than upper surfaces of the first and second gate electrodes;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[Claim 7]

The semiconductor device according to Claim 6, wherein the gate line has a laminated structure of the metal film and a silicide.

[Claim 8]

The semiconductor device according to Claim 6, wherein the thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the metal film and polysilicon film.

[Claim 9]

The semiconductor device according to Claim 6, wherein the center line of the gate line is displaced from a line that connects a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer by a first predetermined distance.

[Claim 10]

The semiconductor device according to Claim 9, further comprising silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.

Claims

1. A method of producing a semiconductor device, the method which comprises the following:

a first step including forming a planar silicon layer on a silicon substrate, and

forming a first pillar-shaped silicon layer and a second pillar-shaped silicon layer on the planar silicon layer;

a second step, subsequent to the first step, including forming a gate insulating film around each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer,

forming a metal film and a polysilicon film around the gate insulating film, wherein a thickness of the polysilicon film is smaller than half a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer,

forming a resist, and

after forming the resist, forming a gate line by performing anisotropic etching of at least the polysilicon film, and

subsequent to performing the anisotropic etching, removing the resist; and

a third step, subsequent to the second step, including depositing a further resist so that a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer is exposed, removing the exposed portion of the polysilicon film by etching, removing the further resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode, wherein the first gate electrode and the second gate electrode are connected to the gate line.

2. The method for producing a semiconductor device according to claim 1, which comprises etching upper portions of the first pillar-shaped silicon layer and second pillar-shaped silicon layer by the anisotropic etching.

3. The method for producing a semiconductor device according to claim 1, wherein an upper surface of the resist for forming the gate line is located at a lower position than an upper surface of the polysilicon film on each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer.

4. The method for producing a semiconductor device according to claim 1, further comprising a fourth step including forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer,

forming a second n-type diffusion layer in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer,

forming a first p-type diffusion layer in an upper portion of the second pillar-shaped silicon layer, and

forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

5. The method for producing a semiconductor device according to claim 4, further comprising a fifth step including forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

6. A semiconductor device, comprising:

a planar silicon layer formed on a silicon substrate;

first and second pillar-shaped silicon layers formed on the planar silicon layer;

a gate insulating film formed around the first pillar-shaped silicon layer;

a first gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

a gate insulating film formed around the second pillar-shaped silicon layer;

a second gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

the thickness of each of the polysilicon films being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer;

a gate line connected to the first and second gate electrodes;

an upper surface of the gate line being located at a lower position than upper surfaces of the first and second gate electrodes;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

7. The semiconductor device according to claim 6, wherein the gate line has a laminated structure of the metal film and a silicide.

8. The semiconductor device according to claim 6, wherein the thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the metal film and polysilicon film.

9. The semiconductor device according to claim 6, wherein the center line of the gate line is displaced from a line that connects a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer by a first predetermined distance.

10. The semiconductor device according to claim 9, further comprising silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.

11. The method for producing a semiconductor device according to claim 1, wherein the step of forming the gate line by performing anisotropic etching includes also removing portions of the metal film that are not protected by the resist.