

The invention relates to a circuit arrangement for generating a vertical frequency deflection current for the electron beams in a picture tube of a television set.

In modern television sets, the deflection current is generated with the help of a Class D amplifier in that an electronic switch, which is controlled by pulses that have their width modulated at the line frequency, periodically switches the deflection coils to earth potential via the line transformer. For the regulation of the deflection current therein, there serves an error amplifier whose output is connected to the one input of a pulse width modulator to whose other input there is supplied a horizontal frequency sawtooth signal. The input of the error amplifier lies across the bridge diagonals of a resistance bridge in that the inputs of the error amplifier are each connected via an equally large resistor to a fixed operating voltage and wherein on the other hand, a reference direct voltage potential and a vertical frequency sawtooth signal are applied to the inputs via equally large resistors. In addition, a very low ohmic sensing resistor is connected between the resistors connected to the fixed operating voltage potential (EP 0 074 468 A1). An arrangement of this type has the disadvantage that not only are the bridge resistors and the error amplifier subject to temperature drifts but also, the DC characteristic of the horizontal frequency sawtooth signal and the dynamic response of the switching thyristor enter into the temperature stability. In addition, the components in the circuitry have tolerances which can have a disadvantageous effect on the circuit.

The object of the invention is to eliminate drifts and tolerances of this type so that the stability of the known circuit arrangement is reduced to the thermal stability of the resistance bridge and of the input-offset characteristic of the error amplifier so that the circuit can be implemented as an integrated circuit. This object is achieved by the measures specified in claim 1. Further advantageous embodiments of the invention are apparent from the appendant claims.

The invention will be explained hereinafter on the basis of an embodiment with the help of the drawing.

Figure 1 shows a first embodiment of the invention

Figure 2 shows a second embodiment of the invention.

Firstly, in Figure 1, we are concerned with the known vertical deflection circuit in which, on the one hand, the vertical

deflection coils LV are connected via a current sensing resistor RS that is measuring the deflection current to an operating direct voltage UB and, on the other hand, they can be periodically connected by the controllable electronic switch TH to reference potential via a winding W of the line transformer ZT and an inductance L. The connection of the vertical deflection coils LV to the winding W of the line transformer ZT is connected via an integrating capacitor C2 to earth potential. A reverse poled diode D is connected in parallel with the electronic switch TH. The electronic switch TH is controlled by line frequency pulses which are width modulated so that the times, at which the vertical deflection coils LV are at earth potential, are matched to the deflection angle. The line frequency control pulses are delivered by a pulse width modulator PBM which has two inputs of which the one is connected to a horizontal frequency sawtooth signal UH and the other to the signal from an error amplifier FV. The error amplifier FV has two inputs which are connected between the points A and B of a bridge consisting of the resistors R1, R2, R3 and R4. The resistors R1, R3 are connected to the operating voltage source UB on the capacitor C1, wherein the current sensing resistor RS is arranged therebetween. A fixed reference potential VDC is supplied to the other two arms of the bridge via the resistor R2 on the one hand and a vertical frequency sawtooth signal UV is supplied to the other two arms of the bridge via the resistor R4 on the other hand. The error amplifier FV regulates the width of the pulses and hence the deflection current in such a way that the bridge voltage Ub disappears.

Here, in accordance with the invention, there is utilised a transconductance amplifier which possesses the ability to transform an input voltage that has been fed to it into an output current. In the example, the transconductance amplifier is intended to deliver a current of 1 to 2 mA per 1 V change of the input voltage i.e. it has a g_m of 1 to 2 mA/V. An RC network Ra, Ca having a time constant that is dimensioned such that a complete correction occurs within a few lines is connected to the output of the transconductance amplifier. In a circuit construction that has been tried in practice, an Ra of 33 kohm and a Ca of 15 nF were established. A capacitor Cb connected in parallel with the RC network Ra, Ca filters out residual components of the line frequency. A drift of the horizontal sawtooth signal as well as the drift of the electronic switch is eliminated in this manner. The resistor Ra of the RC network Ra, Ca delivers the P component of the PI regulator whereby the stability of the regulation is also ensured.

A further example for the application of the invention is given in Figure 2. The vertical output stage here, is an amplifier which is working in Class A-B. Herein, the one (+) input of the amplifier V is applied to a fixed reference voltage U_{ref} , the signal from the transconductance amplifier FV being connected to the other (-) input of the amplifier V. The same considerations with regard to drift and temperature characteristics as for the arrangement according to Figure 1 also apply to this arrangement.

Claims



1. Circuit arrangement for generating a vertical frequency deflection current for the electron beams in a picture tube of a television receiver including a current sensing resistor (RS) arranged in the deflection current circuit to whose one end there is supplied a direct voltage potential (DC) via two series connected resistors (R1, R2) and to whose other end there is supplied a vertical frequency sawtooth signal (UV) via two series connected resistors (R3, R4), wherein the connecting point (A, B) of the two series connected resistors (R1, R2; R3, R4) are connected to the inputs of an error amplifier (FV) whose output is connected to the input of the output stage delivering the deflection current, characterised in that, the error amplifier (FV) is constructed as a transconductance amplifier whose output is connected via a series circuit of a resistor (Ra) and a capacitor (Ca) to reference potential.
2. Circuit arrangement in accordance with Claim 1, characterised in that, the output stage delivering the deflection current consists of a pulse width modulator (PBM) having an interconnected vertical output stage working in Class D (TH, D) and the output of the transconductance amplifier is connected to the input of the pulse width modulator (PBM).
3. Circuit arrangement in accordance with Claim 1, characterised in that, the output stage delivering the deflection current is constructed as a power output stage working in Class A-B and the output of the transconductance amplifier is connected to the input of the vertical output stage.
4. Circuit arrangement in accordance with Claims 1, 2 or 3, characterised in that, the time constant (T) of the RC network (Ra, Ca) is in the order of magnitude of several lines.