INTEGRATED CIRCUIT PACKAGE SYSTEM WITH RELIEF

TECHNICAL FIELD

The present invention relates generally to integrated circuit package systems, and more particularly to integrated circuit systems with die attach paddles.

BACKGROUND ART

The rapidly growing market for portable electronics devices, e.g. cellular phones, laptop computers, and PDAs, are an integral facet of modern life. The multitude of portable devices represents one of the largest potential market opportunities for next generation packaging. These devices have unique attributes which have significant impacts on manufacturing integration, in that they must be generally small, light weight, and rich in functionality and they must be produced in high volumes at relatively low cost.

As an extension of the semiconductor industry, the electronics packaging industry has witnessed ever-increasing commercial competitive pressures, along with growing consumer expectations and the diminishing opportunities for meaningful product differentiation in the marketplace.

Packaging and materials engineering and development are at the very core of these next generation electronics insertion strategies outlined in road maps for development of next generation products. Future electronic systems may be more intelligent, have higher density, use less power, operate at higher speed, and may include mixed technology devices and assembly structures at lower cost than today.

Current packaging suppliers are struggling to accommodate the high speed computer devices which are projected to exceed one TeraHertz (THz) in the near future. The current technologies, materials, equipment, and structures offer challenges to the basic assembly of these new devices while still not adequately addressing cooling and reliability concerns.

The envelope of technical capability of next generation IC package assemblies are not yet known, and no clear cost effective technology has yet been identified. Beyond the performance requirements of next generation devices, the industry now demands that cost be a primary product differentiator in an attempt to meet profit goals.

The center pad 112, such as a quadrilateral center pad, has center pad sides 114. The center pad 112 is oriented similar to the die pad 106. The relief 110 is surrounded by a wall 116.

The wall 116 in combination with the relief 110 prevents the encapsulation 102 from contaminating the center pad 112. Attached to the center pad 112 and the half-etched bond fingers 104 are external interconnects 118 such as solder bumps. The external interconnects 118 are not on the center pad sides 114 in the relief 110.

Referring now to FIG. 2, therein is shown a cross sectional view of the integrated circuit package system 100 along the line 2--2 of FIG. 1. The integrated circuit package system 100 is shown in greater detail having an integrated circuit die such as a wire-bonded die 202 with an active side 204 above the die pad 106.

The active side 204 of the wire-bonded die 202 is connected to the half-etched bond fingers 104 with bond wires 206. The wire-bonded die 202 is attached to a top surface 208 of the die pad 106 with a die attach adhesive 210. The relief 110 is shown having a flat surface 212.

The wall 116 of FIG. 1 prevents the encapsulation 102 from contaminating the center pad 112 at the bottom 108 of the die pad 106 as described above. The relief 110 physically defines an inner sidewall 221 of the wall 116 and a pad sidewall 223 of the center pad 112. The inner sidewall 221 directly faces the pad sidewall 223. The wall 116 includes an outer sidewall 219 on a side of the wall 116 facing opposite to the inner sidewall 221. The wall 116 prevents the encapsulation 102 from reaching the center pad 112. The center pad 112, the bottom 108, the inner sidewall 221 and the relief 110 are entirely exposed from the encapsulation 102. The encapsulation 102 is shown encapsulating the wire-bonded die 202 and the bond wires 206. A die sidewall 201 of the wire-bonded die 202 is between the inner sidewall 221 and the pad sidewall 223. Below the center pad 112 and the half-etched bond fingers 104, the external interconnects 118 are attached.

Referring now to FIG. 3, therein is shown a bottom view of an integrated circuit package system 300 in a second embodiment of the present invention. The integrated circuit package system 300 is shown having an encapsulation 302, such as an EMC.

The encapsulation 302 is shown encapsulating half-etched bond fingers 304 and a die pad 306 having a bottom 308, and sides 309. The half-etched bond fingers 304 and the die pad 306 may be made from copper or a PPF such as gold, palladium, and nickel.

The bottom 308 of the die pad 306 has a relief 310 etched partially through the die pad 306. The relief 310 is a half-etched portion of the bottom 308 of the die pad 306. The relief 310 surrounds a center pad 312 in the bottom 308 of the die pad 306.

The center pad 312, such as a circular center pad, has one center pad side 314. The relief 310 is surrounded by a wall 316. The different configurations of the center pad 312 enable the integrated circuit package system 300 to be mounted to specialized connections on motherboards, substrates, or memory modules.

The wall 316 in combination with the relief 310 prevents the encapsulation 302 from contaminating the center pad 312. Attached to the center pad 312 and the half-etched bond fingers 304 are external interconnects 318 such as solder bumps. The external interconnects 318 are not on the center pad side 314 in the relief 310.

Referring now to FIG. 4, therein is shown a bottom view of an integrated circuit package system 400 in a third embodiment of the present invention. The integrated circuit package system 400 is shown having an encapsulation 402, such as an EMC.

The encapsulation 402 is shown encapsulating half-etched bond fingers 404 and a die pad 406 having a bottom 408, and sides 409. The half-etched bond fingers 404 and the die pad 406 may be made from copper or a PPF such as gold, palladium, and nickel.

The bottom 408 of the die pad 406 has a relief 410 etched partially through the die pad 406. The relief 410 is a half-etched portion of the bottom 408 of the die pad 406. The relief 410 surrounds a center pad 412 in the bottom 408 of the die pad 406.

The center pad 412, such as a quadrilateral center pad, has center pad sides 414 and rounded corners 415. The center pad 412 is oriented similar to the die pad 406. The relief 410 is surrounded by a wall 416.

The different configurations of the center pad 412 enable the integrated circuit package system 400 to be mounted to specialized connections on motherboards, substrates, or memory modules.

The wall 416 in combination with the relief 410 prevents the encapsulation 402 from contaminating the center pad 412. Attached to the center pad 412 and the half-etched bond fingers 404 are external interconnects 418 such as solder bumps. The external interconnects 418 are not on the center pad sides 414 in the relief 410.

Referring now to FIG. 5, therein is shown a bottom view of an integrated circuit package system 500 in a fourth embodiment of the present invention. The integrated circuit package system 500 is shown having an encapsulation 502, such as an EMC.

The encapsulation 502 is shown encapsulating half-etched bond fingers 504 and a die pad 506 having a bottom 508, and sides 509. The half-etched bond fingers 504 and the die pad 506 may be made from copper or a PPF such as gold, palladium, and nickel.

The bottom 508 of the die pad 506 has a relief 510 etched partially through the die pad 506. The relief 510 is a half-etched portion of the bottom 508 of the die pad 506. The relief 510 surrounds multiple center pads 512 in the bottom 508 of the die pad 506.

The multiple center pads 512, such as quadrilateral multiple center pads, have center pad sides 514. The multiple center pads 512 are oriented similar to the die pad 506. The relief 510 is surrounded by a wall 516.

The different configurations of the multiple center pads 512 enable the integrated circuit package system 500 to be mounted to specialized connections on motherboards, substrates, or memory modules.

The wall 516 in combination with the relief 510 prevents the encapsulation 502 from covering the multiple center pads 512. Attached to the multiple center pads 512 and the half-etched bond fingers 504 are external interconnects 518 such as solder bumps. The external interconnects 518 are not on the center pad sides 514 in the relief 510.

Referring now to FIG. 6, therein is shown a cross sectional view of the integrated circuit package system 500 along the line 6--6 of FIG. 5. The integrated circuit package system 500 is shown in greater detail having an integrated circuit die such as a wire-bonded die 602 with an active side 604 above the die pad 506.

The active side 604 of the wire-bonded die 602 is connected to the half-etched bond fingers 504 with bond wires 606. The wire-bonded die 602 is attached to a top surface 608 of the die pad 506 with a die attach adhesive 610. The relief 510 is shown having a flat surface 612.

The encapsulation 502 is shown encapsulating the wire-bonded die 602 and the bond wires 606. Below the multiple center pads 512 and the half-etched bond fingers 504, the external interconnects 518 are attached.

Referring now to FIG. 7, therein is shown a bottom view of an integrated circuit package system 700 in a fifth embodiment of the present invention. The integrated circuit package system 700 is shown having an encapsulation 702, such as an EMC.

The encapsulation 702 is shown encapsulating half-etched bond fingers 704 and a die pad 706 having a bottom 708, and sides 709. The half-etched bond fingers 704 and the die pad 706 may be made from copper or a PPF such as gold, palladium, and nickel.

The bottom 708 of the die pad 706 has a relief 710 etched partially through the die pad 706. The relief 710 is a half-etched portion of the bottom 708 of the die pad 706. The relief 710 surrounds multiple center pads 712 in the bottom 708 of the die pad 706.

The multiple center pads 712, such as circular multiple center pads, have one center pad side 714. The relief 710 is surrounded by a wall 716.

The different configurations of the multiple center pads 712 enable the integrated circuit package system 700 to be mounted to specialized connections on motherboards, substrates, or memory modules.

The wall 716 in combination with the relief 710 prevents the encapsulation 702 from covering the multiple center pads 712. Attached to the multiple center pads 712 and the half-etched bond fingers 704 are external interconnects 718 such as solder bumps. The external interconnects 718 are not on the center pad side 714 in the relief 710.

Referring now to FIG. 8, therein is shown a bottom view of an integrated circuit package system 800 in a sixth embodiment of the present invention. The integrated circuit package system 800 is shown having an encapsulation 802, such as an EMC.

The encapsulation 802 is shown encapsulating half-etched bond fingers 804 and a die pad 806 having a bottom 808, and sides 809. The half-etched bond fingers 804 and the die pad 806 may be made from copper or a PPF such as gold, palladium, and nickel.

The bottom 808 of the die pad 806 has a relief 810 etched partially through the die pad 806. The relief 810 is a half-etched portion of the bottom 808 of the die pad 806. The relief 810 surrounds multiple center pads 812 in the bottom 808 of the die pad 806.

The multiple center pads 812, such as dissimilarly oriented center pads, have center pad sides 814. The center pad sides 814 form a perimeter of each of the multiple center pads 812 that is not parallel to a wall 816 formed at the sides 809 of the die pad 806. The multiple center pads 812 are oriented dissimilar to the die pad 806. The relief 810 is surrounded by the wall 816.

The different configurations of the multiple center pads 812 enable the integrated circuit package system 800 to be mounted to specialized connections on motherboards, substrates, or memory modules.

The wall 816 in combination with the relief 810 prevents the encapsulation 802 from covering the multiple center pads 812. Attached to the multiple center pads 812 and the half-etched bond fingers 804 are external interconnects 818 such as solder bumps. The external interconnects 818 are not on the center pad sides 814 in the relief 810.

Referring now to FIG. 9, therein is shown a bottom view of an integrated circuit package system 900 in a seventh embodiment of the present invention. The integrated circuit package system 900 is shown having an encapsulation 902, such as an EMC.

The encapsulation 902 is shown encapsulating half-etched bond fingers 904 and a die pad 906 having a bottom 908, and sides 909. The half-etched bond fingers 904 and the die pad 906 may be made from copper or a PPF such as gold, palladium, and nickel.

The bottom 908 of the die pad 906 has a relief 910 etched partially through the die pad 906. The relief 910 is a half-etched portion of the bottom 908 of the die pad 906. The relief 910 surrounds multiple center pads 912 in the bottom 908 of the die pad 906.

The multiple center pads 912, such as quadrilateral multiple center pads, have center pad sides 914 and round corners 915. The multiple center pads 912 are oriented similar to the die pad 906. The relief 910 is surrounded by a wall 916.

The wall 916 in combination with the relief 910 prevents the encapsulation 902 from covering the multiple center pads 912. Attached to the multiple center pads 912 and the half-etched bond fingers 904 are external interconnects 918 such as solder bumps. The external interconnects 918 are not on the center pad sides 914 in the relief 910.

Referring now to FIG. 10, therein is shown the integrated circuit package system 900 along the line 10--10 of FIG. 9 in an intermediate barrier adhesion phase of manufacture. The intermediate barrier adhesion phase of manufacture depicts the die pad 906 and the half-etched bond fingers 904 with a barrier 1002 mounted below. The barrier 1002 contacts the bottom 908 of the die pad 906, and isolates the relief 910.

Referring now to FIG. 11, therein is shown the integrated circuit package system 900 of FIG. 10 in a die attach phase of manufacture. The die attach phase of manufacture depicts an integrated circuit die such as a wire-bonded die 1102 with an active side 1104 above the die pad 906. The wire-bonded die 1102 is attached to a top surface 1106 of the die pad 906 is a die attach adhesive 1108.

Referring now to FIG. 12, therein is shown the integrated circuit package system 900 of FIG. 10 in a wire bonding phase of manufacture. The wire bonding phase of manufacture depicts the active side 1104 of the wire-bonded die 1102 connected to the half-etched bond fingers 904 with bond wires 1202.

Referring now to FIG. 13, therein is shown the integrated circuit package system 900 of FIG. 10 in an encapsulation phase of manufacture. The encapsulation phase of manufacture depicts the encapsulation 902 encapsulating the wire-bonded die 1102 and the bond wires 1202. The barrier 1002 is shown isolating the relief 910. This prevents the encapsulation from contaminating the multiple center pads 912 and the half-etched bond fingers 904 ensuring an unobstructed surface on which to continue processing.

It has been unexpectedly discovered that implementing the barrier 1002 allows increased process control and process speed. The barrier 1002 in combination with the wall 916, help protect against flash, or the encapsulation 902 from contaminating the multiple center pads 912. The barrier 1002 in combination with the wall 916 allows the encapsulation 902 to be molded quickly and with greater pressure without concern for the encapsulation 902 contaminating the multiple center pads 912.

Referring now to FIG. 14, therein is shown the integrated circuit package system 900 of FIG. 10 in a barrier detach phase of manufacture. The barrier detach phase of manufacture depicts the bottom 908 of the die pad 906 exposed. The encapsulation 902 does not contaminate the bottom 908 of the die pad 906 or below the half-etched bond fingers 904.

Referring now to FIG. 15, therein is shown the integrated circuit package system 900 of FIG. 10 in a solder bump phase of manufacture. The solder bump phase of

What is claimed is:

1. A method for manufacturing an integrated circuit package system comprising:

providing a die pad with a top and a bottom, the bottom having a wall, a center pad, and a relief having a flat surface, the relief physically defining an inner sidewall of the wall and a pad sidewall of the center pad with the inner sidewall directly facing the pad sidewall, the wall includes an outer sidewall on a side of the wall facing opposite to the inner sidewall;

mounting a barrier under the bottom of the die pad;

mounting an integrated circuit die on the top of the die pad, with a die sidewall of the integrated circuit die between the inner sidewall and the pad sidewall;

encapsulating the integrated circuit die and the die pad with an encapsulation, the encapsulation entirely covering the outer sidewall and wherein the bottom, the inner sidewall, the flat surface of the relief and the center pad are entirely exposed from the encapsulation;

detaching the barrier; and

mounting an external interconnect on the center pad.

2. The method as claimed in claim 1 wherein:

providing the die pad with the center pad includes providing a quadrilateral center pad.

3. The method as claimed in claim 1 wherein:

providing the die pad with the center pad includes providing a circular center pad.

4. The method as claimed in claim 1 wherein:

providing the die pad includes providing quadrilateral multiple center pads.

5. The method as claimed in claim 1 wherein:

providing the die pad includes a pre-plated finish material of gold, palladium, and nickel.

6. A method for manufacturing an integrated circuit package system comprising:

providing a die pad with a top and a bottom, the bottom having a wall, multiple center pads, and a relief with a flat surface , the relief physically defining an inner sidewall of the wall and a pad sidewall of a pad of the multiple center pads with the inner sidewall directly facing the pad sidewall, the wall includes an outer sidewall on a side of the wall facing opposite to the inner sidewall;

mounting a barrier under the bottom of the die pad;

mounting an integrated circuit die on the top of the die pad, with a die sidewall of the integrated circuit die between the inner sidewall and the pad sidewall;

encapsulating the integrated circuit die and the die pad with an encapsulation, the encapsulation entirely covering the outer sidewall and wherein the bottom, the inner sidewall, the flat surface of the relief and the multiple center pads are entirely exposed from the encapsulation;

detaching the barrier; and

mounting a solder bump on each of the multiple center pads.

7. The method as claimed in claim 6 wherein:

providing the die pad with the multiple center pads includes providing quadrilateral multiple center pads, circular multiple center pads, or quadrilateral multiple center pads.

8. The method as claimed in claim 6 wherein:

mounting the integrated circuit die on the die pad includes mounting a wire-bonded die with an active side and attached with a die attach adhesive.

9. The method as claimed in claim 6 further comprising:

providing half-etched bond fingers; and wherein:

mounting the solder bump includes mounting the solder bump below the half-etched bond fingers; and

connecting the integrated circuit die includes connecting the integrated circuit die with bond wires to the half-etched bond fingers..

10. The method as claimed in claim 6 wherein: mounting the solder bump includes the pad sidewall exposed from the solder bump..

11. An integrated circuit package system comprising:

a die pad with a top and a bottom, the bottom having a wall, a center pad, and a relief having a flat surface, the relief physically defining an inner sidewall of the wall and a pad sidewall of the center pad with the inner sidewall directly facing the pad sidewall, the wall includes an outer sidewall on a side of the wall facing opposite to the inner sidewall;

an integrated circuit die mounted on the top of the die pad, with a die sidewall of the integrated circuit die between the inner sidewall and the pad sidewall;

an encapsulation formed on the integrated circuit die and the die pad, the encapsulation entirely covering the outer sidewall and wherein the bottom, the inner sidewall, the flat surface of the relief and the center pads are entirely exposed from the encapsulation; and

an external interconnect mounted on the center pad.

12. The system as claimed in claim 11 wherein:

the center pad is a quadrilateral center pad.

13. The system as claimed in claim 11 wherein:

the center pad is a circular center pad.

14. The system as claimed in claim 11 wherein:

the die pad includes quadrilateral multiple center pads.

15. The system as claimed in claim 11 wherein:

the die pad includes a pre-plated finish material of gold, palladium, and nickel.

16. The system as claimed in claim 11 wherein: the die pad includes multiple center pads; and the external interconnect is a solder bump.

17. The system as claimed in claim 16 wherein:

the multiple center pads are quadrilateral multiple center pads, circular multiple center pads, or quadrilateral multiple center pads.

18. The system as claimed in claim 16 wherein:

the integrated circuit die mounted on the top of the die pad is a wire-bonded die with an active side and attached with die attach adhesive.

19. The system as claimed in claim 16 further comprising:

a bond finger;

a bond wire between the integrated circuit die and the bond finger; and wherein:

the solder bump is mounted below the bond finger.

20. The system as claimed in claim 16 wherein:

the solder bump is mounted to each of the multiple center pads and the pad sidewall is exposed from the solder bump.