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Description

Semiconductor body with solder material layer ✓

5 The invention relates to a semiconductor body which is composed of silicon and can be soldered to a metal mount via a sequence of metal layers which, prior to soldering, contains, starting from silicon in the direction of the mount, an aluminium layer and a diffusion barrier layer.

10 Such semiconductor bodies are fitted in semiconductor components, in particular in power semiconductor components, which are commercially available in large numbers. The sequence of metal layers generally contains an aluminium layer seated on a silicon semiconductor body. The aluminium layer adheres well to
15 silicon and forms a satisfactory resistive contact particularly with p-doped silicon. According to the prior art, the aluminium layer has seated on it a diffusion barrier layer, which is usually composed of titanium or chromium and serves as adhesion promoter and rear side
20 barrier between a nickel layer, which is seated on the diffusion barrier layer, and the aluminium layer. According to the prior art, a noble metal layer is applied to the nickel layer directly or to a thin titanium layer which follows it and serves to improve adhesion, which
25 noble metal layer is usually composed of silver, gold or palladium and serves as oxidation protection for the nickel layer.

30 In the actual soldering operation, a soldering lamina, which is usually composed of tin and a flux, is generally placed between the rear side, metallized in this way, of the semiconductor body and the metal mount. During the soldering operation, the solder layer inserted between the mount and the silver layer of the semiconductor body then melts, the silver layer
35 dissolving and the following nickel layer being partially dissolved by the soldering material and the soldered joint being produced.



However, this generally known soldering method has serious disadvantages. On the one hand, the different thermal expansion coefficients of nickel and the silicon semiconductor body cause mechanical stresses which lead to severe wafer buckling (buckling $> 1000 \mu\text{m}$), particularly in the case of thin semiconductor bodies (thickness $\leq 250 \mu\text{m}$).

This makes the "handling" of the wafers more difficult, more cassette positioning errors occur and there is increasingly a risk of breaking when the wafers are processed.

This problem has been combatted to date by attempting to minimize the nickel layer thickness to an extent such that the soldering still exhibited sufficient adhesive strength. However, despite a reduced nickel layer thickness ($\approx 1 \mu\text{m}$), nevertheless wafer buckling of 700 to 2000 μm continues to occur in the course of production, and leads to the abovementioned problems.

The object of the present invention, therefore, is to metallize a silicon semiconductor body in such a way that the wafer buckling is distinctly reduced without losses being incurred in the process in terms of the adhesive strength on the mount materials.

This object is achieved by virtue of the fact that a solder material layer is applied to the diffusion barrier layer of a silicon semiconductor body of the type mentioned in the introduction.

A tin or lead or gallium layer is preferably provided as the solder material layer.

Such a semiconductor body is then typically soldered onto the metal mount by applying it to the mount and soldering it directly, that is to say without the addition of further soldering agents and fluxes, to the mount by heating to temperatures above approximately 250°C.

This produces virtually stress-free solder layers, which result in substrate buckling of less than 300 μm . Furthermore, the adhesive strength of the soldered semiconductor bodies on the mounts is very high,

that is to say in regions of greater than 30 MPa. Moreover, embrittlement owing to temperature change loading does not occur, since the metallic phases are only made thin. Overall, the problems in "handling" the wafers and
5 the risk of breaking are consequently eliminated.

Furthermore, a significant cost reduction can be achieved with the semiconductor bodies metallized according to the invention and with the method according to the invention, since the material costs are reduced, in
10 particular due to the omission of an oxidation protection layer, and the throughput can be increased. Moreover, the method according to the invention is also particularly environmentally friendly, since cleaning steps using CFC solvents are dispensed with as a result of the lack of
15 fluxes.

The figure shows the layer sequence of the metals prior to soldering. According to the invention, an aluminium layer 3 is applied to the semiconductor body 1, which aluminium layer adheres well to silicon and forms
20 a satisfactory resistive contact particularly with p-doped silicon. The aluminium layer 3 has seated on it a diffusion barrier layer 4, which is composed of chromium or titanium with a thickness of approximately 50 nm. This layer is either sputtered directly onto the aluminium layer 3 or is directly vapour-deposited. There is
25 applied to the diffusion barrier layer 4 an adhesion promoter layer, e.g. Cu, (not shown) or the solder material is directly applied. The solder layer is composed [sic] either of tin, gallium or lead and is [sic] a
30 thickness of 1000 to 3000 nm, typically a thickness of approximately 2700 nm when tin is used. The silicon semiconductor body 1 metallized in this way is then pressed onto the metal mount 2, which is generally composed of copper, and is joined thereto at
35 approximately 300°C under a protective gas atmosphere or under vacuum conditions, a metal-lurgical connection being produced between the diffusion barrier layer 4, the solder material layer 5 and the mount 2, which is stable up to a temperature of approximately 450°C.

Application of the method according to the invention produces a product of high quality since the layer sequence described results in a particularly good mechanically and electrically stable contact. In particular, the method should be portrayed as very advantageous compared with the prior art both from technological and economical and ecological standpoints.

In technological terms, the method according to the invention opens up the possibility of further reducing the thicknesses of the silicon semiconductor substrates, which leads to an improvement in the conducting-state properties of power semiconductor components. Economically, the advantages are that the material costs can be reduced and the manufacturing throughput can be increased. Finally, the ecological advantage of the method according to the invention resides in the fact that soldering is carried out without fluxes, with the result that it is thereby possible to avoid cleaning steps using CFC-containing solvents.



Patent Claims



1. Semiconductor body (1) which is composed of silicon and can be soldered to a metal mount (2) via a sequence of metal layers which, prior to soldering,
5 contains, starting from the silicon in the direction of the mount, an aluminium layer (3) and a diffusion barrier layer (4), characterized in that a solder material layer (5) is applied to the diffusion barrier layer.
2. Semiconductor body according to Claim 1,
10 characterized in that a tin or lead or gallium layer is provided as the solder material layer (5).
3. Semiconductor body according to either of Claims 1 and 2, characterized by a thickness of the diffusion barrier layer (4) of about 50 nm.
- 15 4. Semiconductor body according to one of Claims 1 to 3, characterized by a thickness of the solder material layer of less than 3000 nm.
5. Method for soldering a semiconductor body (1) according to one of Claims 1 to 5 [sic] onto a metal
20 mount (2), characterized in that the semiconductor body (1) is applied to the mount (2) and is soldered directly to the mount (2) by heating to temperatures above approximately 250°C.

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