

ABSTRACT OF THE DISCLOSURE

A semiconductor wafer surface flattening apparatus achieves stable polish characteristics while maintaining a high throughput value and a small footprint. When an index table 22 rotates by a prescribed angle and indicates a rotation position, a first pre-polish semiconductor wafer is moved to a position near a first platen 23. First through third platens 23 through 25 are installed around the index table 22. First through third carriers 46 through 48 are installed for the platens 23 through 25. One of the carriers 46 through 48 is positioned above each of the platens, respectively. The first carrier above the first platen holds and transports the first pre-polish semiconductor wafer. Then the first pre-polish semiconductor wafer is polished. While the first semiconductor wafer is being polished, a second pre-polish semiconductor wafer is supplied to the index table 22. When the index table 22 rotates by the prescribed angle and indicates another rotation position, the second pre-polish semiconductor wafer is moved to a position near the second platen. After this, the second carrier positioned above the second pre-polish semiconductor wafer picks up, holds, and transports the second pre-polish semiconductor wafer to the second platen. Then the second pre-polish semiconductor wafer is polished. In this way, multiple semiconductor wafers are sequentially polished.

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