

- 1 -

CONTROLLING CONTRAST IN A DIGITAL TELEVISION RECEIVER

5 This invention relates to a circuit and a method for controlling the contrast in a digital television receiver, in which the level of a composite video signal is converted such that a pedestal value of the composite video signal has a zero level.

10 In general, the contrast control in a digital television receiver refers to controlling the shading (or luminance) of the picture on a screen. In a general analog television receiver, there is a method commonly used for converting the amplitude of the luminance signal by means of adding or subtracting the gain of the image signal
15 component provided from an image amplifier. As far as, however, a digital television receiver which is widely researched nowadays is concerned, it is necessary that the contrast control against a video signal converted into digital signal should be carried out proportionally with
20 respect to the amplitude change of an original composite video signal, and further it should be performed by an operational method which avoids distortion of the composite video signal.

25 The digitalized signal of the video composite signal is in general related to the bit number of an analog-digital (A/D) converter employed to a digital contrast circuit. As illustrated in Figure 1, the signal output of the A/D converter is binarily processed to have
30 top value 101 and bottom value 104, dividing the interval between the top value 101 and bottom value 104 into given levels of n-bit data (in the case of an n-bit A/D converter). For instance, in a digital contrast circuit employing a 4-bit A/D converter, the top value 101 will be
35 of binary 1111 and the bottom value 104 will be of binary

0000 in the straight code. Furthermore, the 2's complement values of each the above values are respectively 00001 for the top value 101 and 10000 for the bottom value 104.

5 In addition, the value of the intermediate level 102 can be described in a given digital value. For example, if the straight code of the n-bit intermediate value 102 is 1000, then the 2's complement code corresponding thereto will be 1000.

10 In this case, a signal portion 107 of luminance signal component of the composite video signal 105, relating to the contrast control, is placed between the pedestal level 103 of the composite video signal 105 and
15 the peak value 106 of the composite video signal. In other words, the luminance signal component relating to the contrast control is a signal portion of the composite video signal excluding the synchronous signal component and the pedestal level 103. Namely, it is the signal
20 between the pedestal level 103 and the top value 101.

 If a method of multiplying the gain of the contrast signal for the entire composite video signal, without using the above mentioned method, is used for controlling
25 the contrast signal, then the level of the synchronous signal and pedestal signal component are also multiplied with the same ratio as the contrast signal component, which causes distortion of the composite video signal. Figure 2B shows distortion of the composite video signal
30 against the original composite video signal of Figure 2A.

 Of the distorted composite video signals illustrated in the drawings, distortion of the synchronous signal component may be avoided by suppressing the
35 multiplication during the synchronous signal by means of

a control gate. Nevertheless, the distortion of the DC component of the pedestal level 103 can not be avoided. Accordingly, it is of great necessity to stabilize the pedestal signal level excluding the distortion of the original composite video signals, controlling independently only the signal component relating to the contrast signals.

Accordingly, specific embodiments of the present invention aim to provide a circuit for selectively processing only the contrast signal component of a composite video signal and a method for the same.

Specific embodiments of the invention further aim to provide a circuit for mixing the processed contrast signal with the original composite video signal, thereby to minimise distortion in the video signal.

According to a first aspect of the present invention there is provided a circuit for controlling contrast in a digital television receiver, the circuit comprising:

separating means to separate a luminance signal from a composite video signal, processing means to delay the luminance signal by a predetermined time period, adjusting means to adjust a pedestal level of said luminance signal to be at zero level, and mixing means arranged to mix the processed and adjusted luminance signals together.

Preferably, said separating means comprises a chrominance/luminance signal separator coupled to an analog-digital converter, for separating chrominance signal and luminance signal from a digital composite video signal,

said adjusting means comprises:

5 (i) a level converter coupled to said chrominance/luminance signal separator, for converting said pedestal level of said luminance signal to be at zero level, in response to a reference value applied thereto through a reference pedestal level terminal; and

10 (ii) a gain controller for controlling the output gain of said level converter in response to a gain control value input;

15 said processing means comprises a delay controller for delaying by the predetermined time period the luminance signal output from said chrominance/luminance signal separator;

20 said mixing means comprises a mixer for mixing the outputs of said delay controller and said gain controller in response to a synchronous signal; and

25 said circuit further comprises an overflow detecting and outputting means for detecting an overflow from the output of said mixer so that if the overflow is detected, the overflow detection value is restricted to a maximum value.

Preferably, said level converter comprises:

30 a first adder having at least two input terminals for receiving the output of said chrominance/luminance signal separator, for adding input signals applied to said at least two input terminals in response to a carry signal;

35

a second adder having at least two input terminals for receiving the pedestal value applied through said reference pedestal level terminal, for adding the input signals applied to said two input terminals; and

means coupled so as to compare the respective most significant bits of the signals applied through the two input terminals of said first adder, for determining the sign.

The mixer may comprise:

flip-flop means for providing the output of said gain controller in response to a system clock signal input; and

adding means for adding the outputs of said flip-flop means and said delay controller.

The overflow detecting and outputting means may comprise:

means coupled for detecting an overflow generated from the output of said mixer to produce an overflow signal; and

means for restricting the signal output of said mixer to a maximum value in response to said overflow signal.

According to a second aspect of the present invention, a method of controlling contrast in a digital television receiver is provided, the method comprising:

separating a luminance signal from a composite video signal, processing said luminance signal by delaying said luminance signal by a predetermined time period, adjusting

a pedestal level of said luminance signal to be at zero level, and then mixing the processed and adjusted luminance signals together.

5 The invention also includes a television system which includes a circuit as substantially described with reference to the accompanying drawings.

10 For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

15 Figure 1 shows a waveform of general composite video signals;

 Figures 2A and 2B show waveforms for explaining the distortion of the composite video signals;

20 Figure 3 shows a system block diagram of a circuit for controlling the contrast signal according to one embodiment of the present invention;

25 Figure 4 shows a detailed circuit diagram of a level converter in Figure 3.

 Figure 5 shows a detailed circuit diagram of a mixer in Figure 3.

30 Figure 6 shows a detailed circuit diagram of an overflow detection and output section in Figure 3.

35 A preferred embodiment will now be described in detail with reference to the drawings attached hereto only by way of example.

Referring to Figure 3, an A/D converter 30 converts analog video composite signals provided through an input terminal I₁ thereof into digital signals of n-bit composite video signal to provide the converted digital signals to
5 a chrominance/luminance signal separator 40. Then, the chrominance/luminance signal separator 40 receiving the output of the A/D converter 30 separates the chrominance signal and luminance signal from the digital composite video signal. In addition, the luminance signal output
10 from the chrominance/luminance signal separator 40 is converted by a level converter 60 such that the pedestal level of the composite video signal is to be zero level according to a reference value input from a reference pedestal level terminal 61. The converted signal output is
15 applied to a gain controller 70 which controls the gain of the signal input according to a gain control value input provided through a gain control terminal 62 thereof. In the meantime, the luminance signal output from the chrominance/luminance signal separator 40 is delayed by a
20 predetermined time by a delay controller 50 so as to match the luminance signal with the signal processed by the level converter 60 and the gain controller 70.

The outputs of the delay controller 50 and the gain
25 controller 70 are mixed by a mixer 80 according to a synchronous signal provided from a synchronous signal input terminal 63. The mixed signal is applied to an overflow detection and output section 90 to detect overflow and restrict the detected value to a maximum
30 value, thereby providing the luminance signals free of distortion.

Referring to Figure 4, there is illustrated a detailed circuit diagram of the level converter 60 of
35 Figure 3 which employs the 2's complement code system. In

the drawing, of first to fourth input terminals H_1 , H_2 , L_1 , L_2 of first and second adders ADD_1 , ADD_2 , the first and the third input terminals H_1 , L_1 are coupled to the output of the chrominance/luminance signal separator 40 to receive the luminance signal, and the second and the fourth input terminals H_2 , L_2 thereof are coupled to the reference pedestal level terminal 61 to receive the reference data input. The signals applied to the first and the second adders ADD_1 , ADD_2 are added together and the most significant bits (MSB) of the first and the second input terminals H_1 , L_1 are respectively applied to an OR gate OR_1 so as to obtain a sign-bit of them.

Referring to Figure 5, it shows a detailed circuit diagram of the mixer 80 of Figure 3, in which a data input terminal D of a D-type flip-flop DF is coupled to the output terminal 82 of the gain controller 70, a synchronous signal input terminal 63 is coupled to a clear terminal of the D-type flip-flop DF, and the output terminal Q of the D-type flip-flop DF and the output terminal 81 of the delay controller 50 are respectively coupled to the input terminals of a third adder ADD_3 .

Referring to Figure 6, it shows a detailed circuit diagram of the overflow detection and output section 90 of Figure 3, in which input terminals of a multiplexer MUX and an overflow detection circuit 91 are commonly coupled to the output terminal 83 of the mixer 80, the output of the overflow detection circuit 91 is coupled to a selection terminal S of the multiplexer MUX, and the maximum and minimum input terminals +MAX, -MAX of the multiplexer MUX are respectively controlled to have predetermined values.

Now referring to Figs. 1 through 6, the operation of a preferred embodiment will be described in detail. First of all, the composite video signal input in the form of Figure 1 is digitalized by the A/D converter 30. As mentioned before, in the relation between the analog composite video signal and the digitalized composite video signal, only the value between the pedestal level 103 and the top level 101 is concerned with controlling the contrast of the composite video signal. As usual, in digital signal processing, the amplification of a signal is implemented by multiplication, during which distortion of the composite video signal may occur. In order to avoid distortion of the video signal, it is necessary that the pedestal level should be excluded from the multiplication of the video signal.

In general, when the digital luminance signal is separated by the chrominance/luminance signal separator 40 after being digitalized by the A/D converter- 30, the pedestal level will have a specific level higher or lower than zero level. Therefore, as shown in Figs. 2A and 2B, if the video signal is multiplied by a given gain value, the pedestal level will also be changed causing distortion of the video signal. Accordingly, it is required that a level movement for the current pedestal value should be made so as to change the current pedestal level to a zero level (i.e., 0000 in digital data).

In order to accomplish the above level movement, the luminance signal of the composite video signal from the chrominance/luminance signal separator 40 is applied to the level converter 60 so as to convert its level. Namely, the luminance signals of four bits separated by the chrominance/luminance signal separator 40 are applied to the first and the third input terminals H_1 , L_1 of the

first and the second adders ADD_1 , ADD_2 and the reference values of four bits are applied to the second and the fourth terminal H_b , L_b which are the reference pedestal level terminals 65, respectively. Thus, the signal inputs
5 are added according to the status of the carry terminal thereof to change the pedestal level to zero level. In the meantime, the most significant bits of the signals on the first and the second input terminals H_a , H_b are provided to the OR gate OR_1 to determine the sign.

10

If the composite video signal is centered on the intermediate level 102 in 2's complement code as shown in Figure 1, the pedestal level 103 will have a "-" value. In this case, the pedestal level can be moved to zero level
15 by adding a specific value to the entire composite video signal. If the level movement value of the level converter 60 is applied to the gain controller 70, then the gain controller 70 will multiply the input value by the gain so that only the amplitude of the contrast signal component
20 is changed, keeping the pedestal value at zero level.

The outputs of the gain controller 70 and the delay controller 50 are applied to the mixer 80, in which the delay controller 50 delays by a predetermined time the
25 luminance signal, which is separated by the chrominance/luminance signal separator 40, by using a plurality of delays which are implemented by the D-type flip-flops.

30 The mixer 80, as illustrated in Figure 5, is such constructed that the output of the delay controller 50 is applied to the third adder ADD_3 and the output of the gain controller 70 is applied to the data input terminal D of the D-type flip-flop DF, so that the outputs of the delay
35 controller 50 and the gain controller 70 are latched in

response to the clock pulse from the system clock terminal
SYS-CLK. In addition, the D-type flip-flop DF is cleared
according to the synchronous signal input from the
synchronous signal input terminal 63 and the output of the
5 D-type flip-flop DF is applied to an input terminal of the
third adder ADD, to be added to the output of the delay
controller 50. Such processed data output of the third
adder ADD, is applied to the overflow detection and output
section 90.

10 The overflow detection and output section 90 is
constructed as illustrated in Figure 6, in which a
overflow detection circuit 91 detects an overflow
generated from the output of the mixer 80 and, at the same
15 time, the output of the mixer 80 is applied to the
multiplexer MUX. The multiplexer MUX is controlled under
the detection signal output of the overflow detection
circuit 91 to select the maximum value, minimum value, or
normal output.

20 Namely, the contrast signal processed through the
level converter 60 and the gain controller 70 and the
contrast signal delayed by the delay controller 50 are
mixed (added) at the mixer 80 so that the resultant
25 contrast signal is controlled to have an amplitude between
0 and +2. Furthermore, in order to secure the synchronous
signal, the D-type flip-flop DF produces zero value while
the contrast signal is mixed with the gating pulse input,
which is generated in a given time interval through the
30 terminal 63 so that at this time only the contrast signal
may pass through. In the meantime, from such mixed signal,
the signal portion with the overflow is limited at the
overflow circuit 91 as the maximum value. Therefore, the
contrast signal can be properly controlled ~~avoiding~~ the
35 distortion of the composite video signal.

As described above, the contrast signal is processed separately from the original composite video signal and the pedestal level of the contrast signal is converted to be at zero level. Thereafter, such processed
5 contrast signal is mixed with the original composite video signal. It is therefore an advantage of the invention that the distortion of the composite video signal is minimized and the characteristic of the contrast control is enhanced.

10

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that modifications in detail may be made without departing from
15 the scope of the invention.



CLAIMS:

1. A circuit for controlling contrast in a digital television receiver, the circuit comprising:

5

separating means to separate a luminance signal from a composite video signal, processing means to delay the luminance signal by a predetermined time period, adjusting means to adjust a pedestal level of said luminance signal to be at zero level, and mixing means arranged to mix the processed and adjusted luminance signals together.

10

2. A circuit according to claim 1, wherein

15 said separating means comprises a chrominance/luminance signal separator coupled to an analog-digital converter, for separating chrominance signal and luminance signal from a digital composite video signal;

20 said adjusting means comprises:

(i) a level converter coupled to said chrominance/luminance signal separator, for converting said pedestal level of said luminance signal to be at zero level, in response to a reference value applied thereto through a reference pedestal level terminal; and

25

(ii) a gain controller for controlling the output gain of said level converter in response to a gain control value input;

30

said processing means comprises a delay controller for delaying by the predetermined time period the



- 14 -

luminance signal output from said chrominance/luminance signal separator;

5 said mixing means comprises a mixer for mixing the outputs of said delay controller and said gain controller in response to a synchronous signal; and

10 said circuit further comprises an overflow detecting and outputting means for detecting an overflow from the output of said mixer so that if the overflow is detected, the overflow detection value is restricted to a maximum value.

15 3. A circuit as claimed in Claim 2, wherein said level converter comprises:

20 a first adder having at least two input terminals for receiving the output of said chrominance/luminance signal separator, for adding input signals applied to said at least two input terminals in response to a carry signal;

25 a second adder having at least two input terminals for receiving the pedestal value applied through said reference pedestal level terminal, for adding the input signals applied to said two input terminals; and

30 means coupled so as to compare the respective most significant bits of the signals applied through the two input terminals of said first adder, for determining the sign.

4. A circuit as claimed in Claim 2 or 3, wherein said mixer comprises:



- 15 -

flip-flop means for providing the output of said gain controller in response to a system clock signal input; and

5 adding means for adding the outputs of said flip-flop means and said delay controller.

5. A circuit as claimed in any of Claims 2, 3 or 4, wherein said overflow detecting and outputting means comprises:

10 means coupled for detecting an overflow generated from the output of said mixer to produce an overflow signal; and

15 means for restricting the signal output of said mixer to a maximum value in response to said overflow signal.

6. A circuit substantially as herein described with reference to the accompanying drawings.

20 7. A method of controlling contrast in a digital television receiver, the method comprising:

25 separating a luminance signal from a composite video signal, processing said luminance signal by delaying said luminance signal by a predetermined time period, adjusting a pedestal level of said luminance signal to be at zero level, and then mixing the processed and adjusted luminance signals together.

30 8. A method substantially as herein described with reference to the accompanying drawings.



- 16 -

9. A television system including a circuit substantially as herein described with reference to the accompanying drawings.
