

**FORMING FUNCTIONALIZED CARRIER STRUCTURES WITH
CORELESS PACKAGES**

BACK GROUND OF THE INVENTION

5 As semiconductor technology advances for higher processor performance, advances in packaging architectures may include coreless bumpless build-up Layer (BBUL-C) package architectures and other such assemblies. Current process flows for BBUL-C packages involve building of the substrate on a temporary core/carrier capped with copper foil, which is etched off after the package is separated from the core.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

 While the specification concludes with claims particularly pointing out and distinctly claiming certain embodiments of the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

15 FIGS. 1a-1h represent methods of forming structures according to an embodiment of the present invention.

 FIGS. 2a-2e represent methods of forming structures according to an embodiment of the present invention.

 FIG. 3 represents a system according to an embodiment of the present invention.

20

DETAILED DESCRIPTION OF THE PRESENT INVENTION

 In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the methods may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the embodiments. It is to be understood that the various
25 embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the embodiments. In addition, it is to be understood that the location or
30 arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the embodiments. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the embodiments is defined only by the appended claims, appropriately interpreted, along with

the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

Methods and associated structures of forming and utilizing a microelectronic structure, such as a package structure, are described. Those methods may comprise Those
5 methods may include attaching a die to a carrier material, wherein the carrier material comprises a top layer and a bottom layer separated by an etch stop layer; forming a dielectric material adjacent the die, forming a coreless substrate by building up layers on the dielectric material, and then removing the top layer carrier material and etch stop layer from the bottom layer carrier material. Methods of the embodiments enable the
10 functionalizing of the carrier material to create functionalized carrier structures, such as an EMI shield, a stiffener, a heat spreader, an inductor and PoP land structures, for example.

FIGS. 1a-1h illustrate embodiments of a method of forming a microelectronic structure, such as a package structure, for example. FIG. 1a illustrates a carrier material 100, 100'. In one embodiment, the carrier material 100 may comprise a multi-layer copper
15 foil that may serve as a carrier, such as a microelectronic die carrier. In other embodiments, the carrier material may comprise any suitable conductive carrier material 100. In an embodiment, the carrier material 100 may comprise two layers, a top layer 100 and a bottom layer 100' as shown, but may comprise one layer or greater than two layers in other embodiments.

20 In an embodiment, the carrier material 100 may comprise two layers of a conductive material, such as but not limited to copper, for example, that may be separated by a thin etching barrier (stop) layer 102. In an embodiment, the etch stop layer 102 may comprise such materials as nickel, for example, but may comprise any such material that may serve to comprise an etch stop layer to facilitate the stopping of an etch between
25 carrier layers. In an embodiment, the etch stop layer 102 may serve to aid in the formation of a cavity 104 (FIG. 1b), especially during an etching process, for example. In an embodiment, a thickness 103 of the bottom carrier material layer 100' may be dictated by the thickness and embedded depth of a die to be embedded into the carrier material 100' in a subsequent assembly step.

30 The cavity 104 may be formed in one layer of the carrier material, such as by removing a portion of the bottom carrier material layer 100'. The cavity 104 may be formed utilizing any suitable removal process, such as an etching process, such as are known in the art. For example, a masking material may be laminated onto the bottom layer

of the carrier material 100' and the carrier material 100' may be patterned to form the cavity 104, wherein a die may be subsequently placed therein. The etch stop layer 102 between the carrier material layers 100, 100' may serve as an etch stop for the cavity 104 formation and may define a flat surface to place the die on to. The cavity 104 as formed
5 may comprise a bottom portion 101 an angled portion 105, and a top portion 107, wherein the top portion comprises a portion of the etch stop layer 102.

In other embodiments, the cavity 104 may be formed, and the bottom portion of the carrier material 100 may remain substantially flat, as in FIG. 1c. In an embodiment, a die, such as a microelectronic die 106, for example, may be attached within the cavity 104
10 (FIG. 1c). In an embodiment, the die 106 may comprise a thin die 106, and may comprise a thickness of below about 150 microns. In an embodiment, the die 106 may be attached to the top portion 107 of the cavity 104. In an embodiment, the die 106 may comprise at least one sidewall 108, a back side 111 and an active side 112. In an embodiment, the back side 111 of the die 106 may be disposed directly on a portion of the etch stop layer 102
15 within the cavity 104. In some cases, an adhesive film (not shown) and/or an attach process may be used to attach the die 106 into the cavity 104 of the carrier material 100'. In an embodiment, the carrier material, such as copper, can be roughened to aid in the attachment of the die 106.

In an embodiment, the adhesive film can be used as a permanent part of a final
20 package to protect the backside 111 of the die 106, to provide a surface for marking, and/or to manage any warpage that may occur within the die 106, for example. In an embodiment, the adhesive may comprise a back-side film (DBF) that may be applied to the back side 111 of the die 106 prior to placement. The DBF may be filled with metallic particles (e.g, copper or silver), for example, to enhance conductivity when subsequently
25 connected to a heat spreader device, such as a micro-channel heat spreader, for example.

A dielectric material 110 may be formed on the carrier material 100' and adjacent the die 106 that is in the cavity 104 of the carrier material 100' (FIG. 1d). In an embodiment, the dielectric material 110 may be formed by a laminating process, for example. The dielectric material 110 may be formed on the bottom portion 101 of the
30 cavity 104, on the angled portion 105 of the cavity 104, and on a portion of the top portion 107 of the cavity 104 of the carrier material 100' that surrounds the die 106. The dielectric material 110 may provide a level plane for a subsequent build-up process. In an embodiment, the carrier material 100' may be roughened prior to lamination to aid with

adhesion to the dielectric material 110.

In an embodiment, vias 113 may be formed in the dielectric material 110 in a die area landing of the die 106, wherein die pads, for example copper die pads, may be exposed on the active side 112 of the die 106 (FIG. 1e). In an embodiment, a semi-additive process (SAP) may be used to form die pad interconnect structures 112 on die pads of the die 106 and a first metal layer 114 may be formed on the dielectric material 110 adjacent the die 106 (FIG. 1f). Subsequent layers may then be formed using standard substrate SAP build-up processing, for example, wherein further dielectric layers 110' and metallization layers 114' may be formed upon each other to form a coreless substrate portion 116 of a coreless package structure 120 by utilizing the buildup process (FIG. 1g). In an embodiment, the coreless package structure 120 may comprise a BBUL coreless package structure 120, and the die 106 may be fully embedded in the coreless package 120 where fully embedded refers as process where die 106 is directly attached to the layer 110' without the cavity 104.

In an embodiment, when the build-up is complete, the top carrier material 100 and the etch stop layer 102 may be removed, exposing the bottom carrier material 100' that is attached to the coreless package structure 120 (FIG. 1h). The carrier material 100' may be chemically treated to reduce future oxidation, in some cases. In an embodiment, the bottom carrier material 100' may be patterned to form at least one functionalized carrier structure 100'. In an embodiment, the functionalized carrier structure 100' may be disposed within a depth 122 of the coreless package structure 120. The functionalized carrier material 100' may be formed to serve various functions. For example, the carrier material 100' that is retained on/within the coreless package 120 may function as a stiffener 100', in an embodiment. The coreless substrate portion 116 may be built up directly on the stiffener/functionalized carrier structure 100', without any externally added macroscopic adhesive attachment, in some cases. In an embodiment, the coreless package substrate 120 may further comprise interconnect structures 125, such as ball grid array (BGA) balls, that may be attached to the package structure 120.

In an embodiment, by adjusting the right material properties, the presence of the carrier material 100' (which may comprise a copper ring in some cases) around the die 106 can alleviate the warpage of the coreless package structure 120. In some prior art coreless BBUL package structures, very small form factor (~12x12 mm) products may be employed. Larger form factor products will benefit by the addition of the stiffener 100' to

the BBUL package structure 120 without adding additional post-packaging cost, since attachment of a stiffener post-package manufacturing will add cost to the package. Thus, the stiffener of the embodiments herein enable the extension of this technology to more cost sensitive markets/architectures, like chipset, and low-z height mobile CPU's, for example. In other embodiments, the carrier material 100' may be functionalized/formed to serve several additional functions, such as but not limited to the formation of a heat spreader, EMI (electro magnetic interference) shielding, etc. In an embodiment, a top surface 115 of the at least one functionalized carrier structure 100' is coplanar with a top surface 113 of the coreless bumpless buildup package 120 and is coplanar with the backside 111 of the die 106.

In another embodiment, a semi-additive process may be used to form die pad interconnect structures 212 on die pads of a die 206 and a first metal layer 214 may be formed on a dielectric material 210 adjacent the die 206 (FIG. 2a). Vias 215 may be formed outside the die area (in a non-die area) to connect to a bottom carrier layer 200', wherein an etch stop layer 202 may be disposed on the bottom carrier layer 200', and wherein a top carrier layer 200 may be disposed on the etch stop layer 202 (FIG. 2a).

Subsequent layers may then be formed using standard substrate SAP build-up methods to form the remainder of the package 220, wherein further dielectric layers 210' and metallization layers 214' may be formed upon each other to form a coreless substrate portion 216 of a coreless package structure 220 by utilizing the buildup process (FIG. 2b). In an embodiment, the coreless package structure 220 may comprise a BBUL coreless package structure 220. In an embodiment, the top layer of the carrier material 200 and etch stop layer 202 may be removed (FIG 2c). The bottom layer 200' may then be patterned to form an inductor structure 201. In an embodiment, a dry film may be laminated on the bottom carrier material layer 200 and subtractive patterning may be done to form the inductor structure 201. Additional chemical treatment or overmolding of epoxy materials may be done to protect the inductor structures 201 from mechanical and environmental damage, in some cases.

FIG. 2d depicts a top view of a spiral inductor structure 201 shown on either side of the die 206 with vias underneath start and finish point to connect them electrically into the package 220 (vias not shown). In another embodiment, after the top layer of the carrier material 200 and the etch stop layer 202 are removed, the carrier material bottom layer 200' may be patterned to form PoP (Package on Package) land structures 203

adjacent the die 206 (FIG. 2e). In an embodiment, a dry film may be laminated on the top layer of the carrier material 200' and subtractive patterning may be performed to form the POP structures 203.

Additional processing may be done to form the desired surface finish on top of the PoP structures 203, in some cases. An advantage of the present embodiment is that a top surface 231 of the POP pads 203 are flush/coplanar with a top surface (backside) 230 of the die 206, which provides for improved Z-height and ability to attach another package to the coreless package structure 220.

FIG. 3 shows a computer system according to an embodiment of the invention.

System 300 includes a processor 310, a memory device 320, a memory controller 330, a graphics controller 340, an input and output (I/O) controller 350, a display 352, a keyboard 354, a pointing device 356, and a peripheral device 358, all of which may be communicatively coupled to each other through a bus 360, in some embodiments.

Processor 310 may be a general purpose processor or an application specific integrated circuit (ASIC). I/O controller 350 may include a communication module for wired or wireless communication. Memory device 320 may be a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a flash memory device, or a combination of these memory devices. Thus, in some embodiments, memory device 320 in system 300 does not have to include a DRAM device.

One or more of the components shown in system 300 may be included in/and or may include one or more integrated circuit packages, such as the package structures including the functionalized carrier material of FIGS. 1h, 2c and 2e for example. For example, processor 310, or memory device 320, or at least a portion of I/O controller 350, or a combination of these components may be included in an integrated circuit package that includes at least one embodiment of a structure, such as the various functionalized carrier material structures presented herein, described in the various embodiments.

These elements perform their conventional functions well known in the art. In particular, memory device 320 may be used in some cases to provide long-term storage for the executable instructions for a method for forming packaged structures in accordance with embodiments of the present invention, and in other embodiments may be used to store on a shorter term basis the executable instructions of a method for forming package structures in accordance with embodiments of the present invention during execution by processor 310. In addition, the instructions may be stored, or otherwise associated with,

machine accessible mediums communicatively coupled with the system, such as compact disk read only memories (CD-ROMs), digital versatile disks (DVDs), and floppy disks, carrier waves, and/or other propagated signals, for example. In one embodiment, memory device 320 may supply the processor 310 with the executable instructions for execution.

5 System 300 may include computers (e.g., desktops, laptops, hand-helds, servers, Web appliances, routers, etc.), wireless communication devices (e.g., cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, camcorders, digital
10 cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games, watches, etc.), and the like.

 Benefits of the embodiments enable a new packaging architecture that can meet design requirements for future mobile/handheld system on a chip (SoC) processors at roughly half the cost of current package architectures. Various embodiments enable the
15 addition of warpage improvement stiffeners, EMI shielding, inductor structures, PoP land structures and heat spreader structures without added post-package manufacturing cost. The POP land structures of the various embodiments have the added benefit of being formed without the need for an interposer to account for the die thickness in the package.

 Prior art process flows for coreless BBUL packages typically involve building of
20 the substrate on a temporary core/carrier capped with copper foil, which is etched off after the package is separated from the core. The embodiments herein include methods to functionalize the carrier material/copper foil on the carrier for uses such as heat spreaders, warpage improvement, electromagnetic interference (EMI) shielding for RF components, creating pads for Package on Package (POP) applications etc. thus reducing cost and
25 increasing throughput.

 Although the foregoing description has specified certain steps and materials that may be used in the method of the present invention, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within
30 the spirit and scope of the invention as defined by the appended claims. In addition, it is appreciated that various microelectronic structures, such as package structures, are well known in the art. Therefore, the Figures provided herein illustrate only portions of an exemplary microelectronic device that pertains to the practice of the present invention.

Thus the present invention is not limited to the structures described herein.

IN THE CLAIMS

What is claimed is:

5

1. A method comprising;

forming a cavity in a carrier material, wherein the carrier material comprises a top layer and a bottom layer separated by an etch stop layer; attaching a die in the cavity;

10

forming a dielectric material adjacent the die and on the carrier material bottom layer;

forming a coreless substrate by building up layers on the dielectric material; and

15

removing the carrier material top layer and etch stop layer from the bottom layer of the carrier material.

2. The method of claim 1 further comprising wherein the bottom layer of the carrier material remains attached to the coreless substrate.

20

3. The method of claim 2 further comprising wherein the bottom layer of the carrier material comprises at least one of a heat spreader, an EMI shield structure, and a stiffener.

25

4. The method of claim 3 further comprising wherein the stiffener comprises a copper ring around the die.

5. The method of claim 1 further comprising removing the carrier material top layer and etch stop layer while they are disposed on the coreless substrate.

30

6. The method of claim 4 further comprising wherein the stiffener is attached to the substrate with no adhesive.

7. The method of claim 1 further comprising wherein the carrier material

comprises copper.

8. The method of claim 1 further comprising wherein the coreless substrate comprises a portion of a coreless, bumpless, build up layer package.

5

9. A method comprising:

attaching a die to a carrier material, wherein the carrier material comprises a top layer and a bottom layer separated by an etch stop layer;

forming a dielectric material adjacent the die and on the bottom layer of the carrier material;

10

forming die pad interconnect structures in the die area;

forming vias in a non-die area to connect with the bottom layer carrier material;

15

forming a coreless substrate by building up layers on the dielectric material; and

removing the top layer carrier material and etch stop layer from the bottom layer carrier material.

20

10. The method of claim 9 further comprising patterning the bottom layer carrier material to form at least one of an inductor and a PoP land structure.

11. The method of claim 9 further comprising wherein the bottom layer carrier material is attached to the coreless package without an adhesive.

25

12. The method of claim 9 wherein the coreless substrate comprises a portion of a coreless, bumpless, build up layer package.

30

13. The method of claim 10 further comprising wherein a top surface of the PoP land structure is coplanar with a top surface of the coreless bumpless buildup package

14. A structure comprising:

a die embedded in a coreless substrate;

a dielectric material adjacent the die;
die pad interconnect structures disposed in a die pad area of the die;
and

5 at least one functionalized carrier structure disposed within the
coreless substrate, wherein a top surface of the at least one functionalized
carrier structure is coplanar with a top surface of the coreless substrate.

15 15. The structure of claim 14 wherein the at least one functionalized structure
comprises a copper material.

10

16. The structure of claim 14 wherein the coreless substrate comprises a
portion of a coreless bumpless buildup package structure.

15 17. The structure of claim 14 wherein the at least one functionalized carrier
structure comprises at least one of a stiffener, a heat spreader and an EMI shield.

18. The structure of claim 14 wherein the functionalized carrier structure is
attached to the coreless package without an adhesive.

20 19. The structure of claim 18 wherein functionalized carrier structure
comprises copper.

25 20. The structure of claim 16 wherein the die is coplanar with a top surface of
the functionalized carrier structure, and wherein the die is fully embedded in the
coreless substrate.

30 21. A structure comprising:
a die embedded in a coreless substrate;
a dielectric material adjacent the die;
die pad interconnect structures disposed in a die pad area of the die;
vias in the coreless substrate disposed in a non-die area that are
connected to a functionalized carrier structure, wherein the functionalized
carrier structure is disposed within the coreless substrate, and wherein a top

surface of the functionalized carrier structure is coplanar with a top surface of the coreless substrate.

- 5 22. The structure of claim 21 wherein the functionalized carrier structure comprises a copper material.
23. The structure of claim 21 wherein the coreless substrate comprises a portion of a coreless bumpless buildup package structure.
- 10 24. The structure of claim 21 wherein the functionalized carrier structure comprises at least one of an inductor and a PoP land structure.
25. The structure of claim 24 wherein a top surface of the PoP land structure is coplanar with a top surface of the coreless bumpless buildup package.
- 15 26. The structure of claim 25 wherein the coreless bumpless buildup package does not comprise an interposer.
27. The structure of claim 24 wherein the at least one inductor comprises at least one spiral inductor adjacent the die, wherein a top surface of the at least one spiral inductor is coplanar with a top surface of the die.
- 20 28. The structure of claim 21 further comprising a system comprising:
 a bus is communicatively coupled to the structure; and
25 a DRAM communicatively coupled to the bus.
29. The structure of claim 21 wherein the die is coplanar with a top surface of the functionalized carrier structure, and wherein the die is fully embedded in the coreless substrate.
- 30 30. The structure of claim 21 wherein the functionalized carrier structure is attached to the coreless package without an adhesive.