PROCESS FOR MAKING A METAL SEED LAYER

This application is a continuation in part of U.S. Patent Application No. 11/331,552, filed January 13, 2006, which claims the benefit of U.S. Provisional Patent Application No. 60/724,953, filed October 6, 2005, both of which are expressly incorporated by reference herein in their entireties. This application also claims the benefit of U.S. Provisional Application No. 60/803,430, filed May 30, 2006, which is expressly incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor fabrication generally, and more specifically to a method for forming a metal cap layer on a metal line.

BACKGROUND

[0002] In a semiconductor integrated circuit (IC) fabrication process, the back end of line (BEOL) processing results in a plurality of interconnects comprising alternating metal (e.g., copper) and inter-layer dielectric (ILD) layers, with vias through the ILD layers connecting the metal layers.

[0003] In a typical BEOL conductive via fabrication process, copper (Cu) gap filling was performed by electrochemical deposition (ECD) in a substrate formed by plasma vapor deposition (PVD) of a Cu seed layer. When applying these techniques to advanced technologies, such as the 45 nanometer node, post ECD bottom voids can be observed within the PVD Cu seed due to seed layer discontinuities. The observed discontinuous seed layer may be caused by thin seed or Cu oxide dissolving when in contact with the acidic ECD solution.

[0004] When exposed to air, a metal surface such as Cu may be oxidized to form a metal oxide, which adversely impacts subsequent processing. For example, the PVD Cu seed layer, when expose to air, is oxidized to form CuO prior to Cu electrochemical deposition (ECD). A typical ECD solution (the electrolyte) is an acid, which contains from about 1% to about 50 % H_2SO_4 or Methanesulfonic acid. In such an acidic solution, Cu oxide is dissolved, and the Cu seed layer might become discontinuous.

[0005] Exposure of metal to air during processing may adversely affect the fabrication process in other ways, such as affecting a metal cap layer. In determining the performance of a BEOL processing technology, a variety of criteria are used, including the maximum current density (Jmax), the line resistance R_s, and the stress migration (SM). As semiconductor IC technology migrates from 90 nanometer technology to smaller feature sizes, the desired maximum current density Jmax increases. Therefore, a method to improve the electromigration (EM) is desired.

[0006] A metal cap layer can be selectively deposited over the exposed metal surfaces. It has been demonstrated that a tenfold improvement of electromigration (EM) performance in the (VxMx, VxMx+1) interconnect can be obtained by selective use of the metal cap on copper lines. One approach includes deposition of a cobalt cap.

[0007] After chemical mechanical polishing (CMP), the cap layer is selectively applied over the metal lines, but not over the dielectric. After CMP, there is copper oxide on top of the copper line, some post CMP residue on the dielectric, and/or organic contamination from the CMP on both the dielectric and the copper surface. To uniformly deposit a selective metal cap layer on the Cu surface, the Cu oxide must be removed. A pre-clean step has been used to remove the copper oxide. One conventional method includes a wet clean process of immersing the wafer in an acidic solution to dissolve Cu oxide. For example, to achieve high selectivity performance (to avoid leakage), a wet clean solution, including H_2SO_4, Citric Acid and a wetting agent, has been applied to the substrate having exposed metal and dielectric surfaces. The H_2SO_4, Citric Acid and wetting agent remove metal oxide on the metal surface, metal residue on the dielectric surface, and organic residues on both the metal and dielectric surfaces.

[0008] However, during Cu oxide removal by the above-described acidic solution, a recess is created, which results in an increase in line resistance. For example, in some cases, after the metal oxide has been removed, a 3% to 5% increase in line resistance R_s has been observed. For example, the line resistance increase for a process including deposition of a cobalt cap has been measured at about 2.4 %. An increase in R_s degrades RC signal delay performance. Also, because the Cu oxide formation can be pattern dependent, differences in the depths of the Cu recess occur on dense and iso pattern areas, resulting in non-uniform metal cap deposition.

SUMMARY OF THE INVENTION

[0009] In some embodiments, a method comprises the steps of: providing a substrate with an exposed metal surface; performing a reducing process on the metal surface; and transferring the substrate in an inert or reducing ambient to a chamber that is used for metal layer deposition.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a diagram showing an exemplary process for electroless deposition of a cap layer above a metal layer on a substrate.

[0011] FIG. 2 is a diagram showing a substrate with an exemplary cap layer having a glue layer and a barrier (passivation) layer.

[0012] FIG. 3 is a histogram comparing the line resistance increase for five variations on a cap deposition process.

[0013] FIG. 4 is a flow chart diagram of one embodiment of the invention.

[0014] FIG. 5 is a flow chart diagram of another embodiment of the invention.

[0015] FIG. 6A shows a via having a seed layer.

[0016] FIG. 6B shows the via of FIG. 6A, after a portion of the metal in the seed layer is dissolved.

[0017] FIG. 7 is a flow chart diagram of an exemplary method.

[0018] FIG. 8 is a flow chart diagram of an example in which an integrated dry-wet process is used to form a seed layer, followed by ECD filling and another dry-wet integrated process to form a cap layer.

DETAILED DESCRIPTION

[0019] This description of the exemplary embodiments is intended to be read in connection with the accompanying drawings, which are to be considered part of the entire written description. In the description, relative terms such as "lower," "upper," "horizontal," "vertical,", "above," "below," "up," "down," "top" and "bottom" as well as derivative thereof (e.g., "horizontally," "downwardly," "upwardly," etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms

are for convenience of description and do not require that the apparatus be constructed or operated in a particular orientation.

[0020] FIG. 6A shows an example of an interconnect structure 600 including via 612 having a continuous seed layer 610 of a metal, such as Cu formed along the sides walls and bottom thereof. Also shown are the underlying dielectric layers 602 and 606, and etch stop layers 604 and 608. The metal of seed layer 610 may have non-uniform thickness. For example, as shown in FIG. 6A, the seed layer 610 may have thinner metal at the bottom of the sidewalls than at the top of the sidewalls.

[0021] FIG. 6B shows the via 612 wherein a portion 610d of the seed layer 610 has dissolved, forming discontinuities in the metal. Such discontinuous metal (Cu) seed degrades the subsequent ECD process to form voids in the feature (via) to cause yield loss.

[0022] One example described below cleans the metal oxide on the exposed continuous metal surface of a substrate, of a type such as the seed layer 610 for a via 612 in the interconnect structure 600, as shown in FIG. 6A. FIG. 7 is a flow chart diagram of an exemplary process.

[0023] One example is described below of a "dry-wet integrated" process for fabricating a via with metal conservation by direct metal oxide reduction for subsequent filler metal deposition. The teachings below are not limited to conductive vias, and may be applied to other features, such as a trench of an isolation structure, or a contact, for example.

[0024] Referring now to FIG. 7, at step 700, an interconnect structure 600 or trench with an exposed metal surface 610 is provided. The exposed metal substrate may be a copper seed layer 610, and may have a portion thereof oxidized by exposure to the ambient air. For example, the substrate may be a Cu seed layer 610 that is at least partially oxidized to form CuO.

[0025] At step 710, a reducing process is performed on the metal surface 610. The oxide is converted to metal (or alloy, if the seed layer is formed of an alloy).

[0026] At step 720 the interconnect structure 600 is transferred in an inert or reducing ambient to a chamber (not shown) that is used for metal layer deposition.

[0027] At step 730, the metal deposition is performed, to fill the via 612 with metal.

[0028] Many embodiments and variations of this process may be performed by those of ordinary skill in the art in accordance with the general process described above.

[0029] The continuous metal substrate is not limited to a Cu material. Other types of seed layers may be used, such as, for example, continuous W, Ru, Co, Ni, Ti, or alloys thereof.

In some embodiments, a barrier metal (e.g., Ta or TaN) underlies the Cu seed layer. In some embodiments, the underlying barrier metal beneath the via is a platable metal such as Co, Ni, Ru or alloy, and there is no need to deposit a separate seed layer. The fill can be deposited directly on the Co, Ni, Ru or alloy. For example, in technologies such as the 22 and 16 nanometer node, it is contemplated that platable barriers may be used without a Cu seed layer, for direct deposition of the via filler metal.

[0030] In the above example, the dry reducing process is performed at a relatively low temperature (e.g., about 25 C to about 200 C) to convert the surface metal oxide to metal, without causing metal agglomeration. For a 45 or 32 nanometer technology device, the seed layer has a thickness from about 5 nanometers to about 30 nanometers. Often, when a metal oxide is reduced, the resulting metal can be porous, and the thickness can increase, interfering with the subsequent electrochemical deposition. By using a low temperature annealing step at about 25 C to about 200 C, and avoiding metal agglomeration, a desired grain structure is achieved throughout the seed layer, and the subsequently deposited metal fill is also deposited with the desired uniform grain structure.

[0031] To transform the metal oxide to metal, an in-situ plasma or downstream plasma may be applied in a vacuum environment. A downstream plasma is preferred, to avoid direct bombardment of the substrate by the plasma. Alternatively, a thermal baking step may be performed in N_2 gas followed by a thermal bake in H_2 or forming gas (including H_2 and N_2). The thermal bake step provides the desired grain structure uniformly throughout the metal substrate 610. The dry reduction process may be performed with or without ultraviolet (UV) or e-beam treatment.

[0032] After the dry reducing process, the interconnect structure 600 including the metal substrate 610 is transferred in an inert (e.g., N_2, Ar or other noble gas) or reducing (e.g., H_2) ambient to a chamber for subsequent metal deposition. In some preferred embodiments, the dry reducing process, the transfer, and the subsequent metal deposition are all performed within a dry and wet integrated cluster tool. The cluster tool maintains the desired inert or reducing ambient in between the dry reducing process chamber and the subsequent (e.g., wet) process chamber.

[0033] After the structure is transferred to the chamber for subsequent processing, the fill operation is performed. For filling a via, a variety of methods may be used for metal deposition including, but not limited to (a) dry process deposition, such as PVD, chemical vapor deposition

(CVD), or atomic layer deposition (ALD); (b) wet process deposition, such as electroplatng, electroless plating, or displacement deposition. If a wet deposition process is used, it is preferred that this process is performed by a "dry-wet" integrated tool.

[0034] If the via or trench is to be filled by an electroless process, then a self activation process is performed. Copper self activation (self initiation) is described further below, in the discussion of table 1. In embodiments where the via or trench is filled by electroplating (electrochemical deposition), there is no need to perform a self-activation process

[0035] The above described example allows void free gap filling for interconnects (vias, trenches, contacts) and can be extended to technology nodes beyond 45 nanometers.

[0036] In some embodiments, the combination of a dry reduction process, transfer in an inert or reducing ambient, and a wet deposition process can be used for forming a cap layer, either alone or in combination with the above-described method for gap filling. An example is described below with reference to FIG. 8.

[0037] First, a process is described for forming a cap layer using a wet-dry integrated process. The process described below enables cleaning the metal oxide on the exposed metal surface, the metal residue on the exposed dielectric surface, and the organic residues on both the metal and dielectric surface, with little or no increase in the line resistance R_s. FIG. 1 is a diagram showing the process and the changes to the structure that occur during the process. FIG. 4 is a flow chart diagram of an exemplary process.

[0038] At step 400 (FIG. 4) a substrate 110 is provided with exposed metal and dielectric surfaces. The exposed metal may be a copper line 120, and may have an oxide layer 122 at its exposed surface. The exposed dielectric of substrate 110 may have a residue 126 thereon.

[0039] At step 410, a reducing process is performed on the metal surface 122 and dielectric surface 110. The oxide 122 and residue 126 are removed.

[0040] At step 420 the substrate 110 is transferred in an inert or reducing ambient to a chamber (not shown) that is used for selective metal layer deposition.

[0041] At step 430, the selective metal layer deposition is performed, to form the metal layer 124.

[0042] FIG. 5 is a flow chart diagram showing one embodiment of the invention.

[0043] At step 500 a substrate 110 is provided with exposed metal and dielectric surfaces.

[0044] At step 510, a reducing process is performed on the metal surface 122 and dielectric surface 110. Preferably, the reducing process is a dry process performed in a dry and vacuum chamber. In some embodiments, the reducing process includes exposing the substrate to an in-situ plasma or a downstream plasma. A plasma that has H_2 or forming gas reduces the copper oxide, without dissolving the copper. Thus, the recess observed in the wet pre-clean process is avoided. A downstream plasma is preferred because it avoids plasma induced damage to the substrate.

[0045] In other embodiments, the reducing process includes a thermal bake in H_2 or a forming gas (including H_2 and N_2). An exemplary thermal baking step may be performed at a temperature from about 100 degrees C to about 400 degrees C. In some embodiments, the temperature is about 200 degrees C.

[0046] If a thermal baking step is used, the substrate may optionally be exposed to an ultra-violet (UV) or electron beam (e-beam).

[0047] At step 520, the substrate 110 is transferred to a chamber in an inert gas (e.g., a noble gas or nitrogen) or a reducing ambient to perform electroless metal cap layer deposition without a wet pre-clean step. In some embodiments, the substrate is placed in an intermediate chamber between the dry clean process and the wet cap deposition process. This prevents the copper oxide from re-forming on the lines.

[0048] In some embodiments, the intermediate chamber is a vacuum or low pressure chamber that is separate from the chamber in which the dry clean process is performed, and separate from the chamber in which the wet deposition process is performed.

[0049] In some embodiments, the dry clean process, the intermediate transfer and the wet deposition are all performed in a cluster tool, and the intermediate chamber is included within the cluster tool.

[0050] At step 525, to make sure that the Cobalt is selectively deposited on copper, and not on the dielectric, a step is performed, in between the surface cleaning and the deposition. Once the substrate has been transferred to the chamber for cap deposition, an activation or initiation step is performed. In some embodiments, the activation or initiation step is a palladium (Pd) activation or Pd initiation. In other embodiments, a step is performed to initiate or activate the copper surface, referred to as the self initiation process.

[0051] Both of the initiation processes involve an electroless process in a solution that is different from the solution used to deposit the cobalt cap. Table 1 lists a variety of solutions that can be used for the self activation and Pd activation processes, before depositing a cobalt cap on copper lines. In Table 1, "DMAB" denotes "Dimethylamine Borane."

Table 1

Selective Co Based Capping Layer Deposition		Co Based, Pd Activated			Co Based, Non-Pd Activated					
Function	Component (example)	Co(P)	Co(W,P)	Co(Mo,P)	Co(B)	Co(P,B)	Co(W,B)	Co(Mo,B)	Co(W,P,B)	Co(Mo,P,B)
Source of Co	Co Salt, CoCl2 orCoSO4	v	V	v	v	v	v	v	v	v
Source of M2 (W or Mo)	(NH4)2WO4, Na2WO4, H3[P(W3O10)4]		V				v		v	
	(NH4)2MoO4, Na2MoO4,			v				v		v
Reduction Agent and source of N (P or B)	NaH2PO2•2 H2O	v	V	v		v			v	v
	NaBH4, (CH3)2NHBH3 (DMAB)				v	v	v	v	v	v
Surface Activation	Pd – Cu displacement dep	v			option					
	Chemical Grafting + Pd ions adsorption	v								
	Chemical Grafting only (non-Pd approach)	v								
Complex Agent	Na3C6H5O7 • 2 H2O	v			v					
Stabilizer	Pyridine, Citric Acid, CrCl3	option			v					
PH	8.5 – 10	v			v					
Dep. Temperature	70 – 80 °C	v			v					
Bath Stability		long			short					

[0052] For the Pd activation process, one of the following processes is used: Pd – Cu displacement deposition or Chemical Grafting with Pd ions adsorption. Chemical grafting is a process of attachment of a low molecular weight active group (monomer) to a parent polymer or membrane. Either bulk polymer or surface modification is possible.

[0053] In the Pd initiation process the Cobalt electroless solutions could grow on the copper. If palladium initiation is used, that palladium layer would form a copper alloy, which would cause further R_s increase.

[0054] The self initiation process involves use of an electroless cobalt solution, having a composition to make the copper surface active enough to act as a catalyst surface, to reduce the cobalt (i.e., to grow the cobalt on the copper). The self initiation process allows the Cobalt deposition process to be used to provide the minimum R_s, because no Pd layer forms on the copper. With a self-initiation process, it's possible to provide a cobalt cap having an R_s increase of about 2% to about 2.4% greater than the Cu line with no cap.

[0055] At step 530, after the self activation or Pd activation, a selective electroless metal cap layer deposition process is performed.

[0056] US Patent Nos. 6495453, 6713377, 6207553 and 6204192 are incorporated by reference herein in their entireties. These patents teach a variety of electroless deposition techniques.

[0057] In some embodiments, the cap material deposited on the copper is an alloy of cobalt tungsten and boron. In other embodiments, the cap material deposited on the copper is an alloy of cobalt, tungsten, boron and phosphorus. Many other cobalt alloys may be used. Preferably, the cap alloy comprises more than 80% cobalt. In some embodiments, the electroless deposition is performed at a temperature of about 65 degrees C to about 95 degrees C.

[0058] Different electroless solution compositions are used to provide the cobalt alloy cap, depending on whether the copper is self-activated or Pd activated. For the palladium initiation a preferred reducing agent includes phosphorous (e.g., $NaH_2PO_2 \cdot 2\ H_2O$), and the alloy of the cap may be a Co(P) alloy, a Co(W,P) alloy, or a Co(Mo,P) alloy. Boron is the most used element for the self activation process. The reducing agent for the self-activation can include boron (e.g., $NaBH_4$, $(CH_3)_2NHBH_3$ (DMAB)) or phosphorous (e.g., $NaH_2PO_2 \cdot 2\ H_2O$), and the alloy of the cap may be a Co(B) alloy, a Co(P,B) alloy, a Co(W,B) alloy, a Co(Mo,B) alloy, a Co(W,P,B) alloy or a Co(Mo,P,B) alloy.

[0059] In performing the electroless deposition, desired properties for a top passivation layer on Cu are different from a layer that is optimized to be deposited below a dielectric for interfacing between the copper and the dielectric. For the interface between the Cu and the cap, a pure metal contact with the Cu is used to provide a good interface and strong bonding. For the interface between the Cu and the ILD above the Cu, grain boundary stuffing is advantageous to enhance the barrier property of the cap.

[0060] At step 535, an optional second cap layer is deposited. FIG. 2 shows an advantageous cap layer provided by: depositing a first layer of near pure metal on the Cu interface; and depositing a second layer as a cap, where the second layer has a highly stuffed grain boundary for good barrier properties, low R_s, and for prevention of plasma damage etching damage, oxidation and Cu diffusion. Thus, the resulting interconnect comprises the first metal layer (e.g., copper), and a cap comprising second and third metal layers. The second metal layer is formed over the first metal layer as a glue layer, and a third metal layer formed over second metal layer as a passivation layer or barrier layer. The second metal layer may include at least about 95 atom % Co or Ni, and the third metal layer may include at most about 95 atom % Co or Ni. In the second and third metal layers, the alloying element includes one or more of the following elements: W, P, Mo, Re, and/or B.

[0061] In one embodiment, the second metal layer is deposited using one chemical, and the third metal layer is deposited by simultaneously changing one or more process parameters. The process parameter that is varied may be, for example, the spin rate (rpm), the flow rate, the chemical concentration, or the temperature of the electroless deposition solution, or a combination of these paramters. For example, in one embodiment, a low temperature liquid is provided on a hot substrate; this creates a multilayer film structure for the beginning and later part of the resulting barrier.

[0062] At step 545, after the electroless deposition, a wet post-deposition cleaning is performed to remove residue particles, for example, using a scrub clean to scrub down the particles.

[0063] Advantageously, the resulting structure can exhibit less than a 1% R_s increase relative to a substrate formed by a process in which there is no wet or dry pre-deposition cleaning step.

[0064] Example

[0065] Samples were tested in a PVD chamber for the process, comparing the line resistance achieved with different pre-deposition cleaning steps. FIG. 3 is a histogram of the data collected.

[0066] All of the samples included a cobalt cap layer. The control sample (labeled "no clean/cap") was fabricated without performing a wet or dry pre-deposition cleaning step. The line resistance of this sample serves as a baseline, against which the line resistance of the other samples are compared. (Although the line resistance of the control sample is better than the other samples, the control sample had a less favorable stress migration performance. Thus, the method disclosed herein is viable compared to the control sample, when the other characteristics Jmax and SM are considered.). The bar labeled "wet clean" represents the prior art wet cleaning acidic solution, having an R_s that is about 2.4% greater than that of the control sample. The bar labeled, "longer wet clean" used a similar process to the "wet clean" bar, with a longer process time, and an even larger increase in R_s.

[0067] The sample using the dry H_2 plasma cleaning before cap deposition had an R_s increase of less than 1% (about 0.8%) above the control sample. The sample using the NH_3 plasma cleaning before cap deposition had an R_s increase of about 1% above the control sample.

[0068] Thus, the method described above can provide a metal cap layer with less than a 1% increase in line resistance relative the sample formed without pre-cleaning. No selectivity is lost, whether the dielectric is of a low K type (e.g., dielectric constant about 2.6) or extra low K type (e.g., dielectric constant of 2.5 or less). The EM performance for both via and trench shows more than a 10X improvement compared to the method without forming the cap over the metal.

[0069] Various embodiments of fabrication methods according to embodiments of the invention are described above. The invention also encompasses a product made by any of the methods described above.

[0070] Although an example is described including a copper metal layer and a cobalt alloy cap, the method described above can be applied to substrates having other types of metal layers thereon, with corresponding compatible cap layers.

[0071] FIG. 8 is a flow chart showing one example of a process in which the above-described dry-wet integrated method is used to form a void-free seed layer, followed by an ECD fill step, and a second dry-wet integrated sequence to form a cap layer.

[0072] At step 800, a seed layer is provided with an exposed continuous metal surface.

[0073] At step 810, a reducing process is performed using an in situ plasma, a downstream plasma, or a thermal bake with or without UV or e-beam treatment.

[0074] At step 820, the substrate is transferred in an inert or reducing ambient at low pressure or vacuum to a chamber for a subsequent ECD..

[0075] At step 830, the ECD filling operation is performed to fill the via.

[0076] At step 840, the top surface of the filled via oxidizes from exposure to air.

[0077] After step 840, steps 510 to 545 (FIG. 5) are performed to form a cap layer over the copper.

[0078] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.

What is claimed is:

1. A method of producing a semiconductor device, comprising:

providing a substrate with an exposed metal surface;

performing a reducing process to reduce the metal surface; and

transferring the substrate in an inert or reducing ambient to a chamber that is used for metal layer deposition.

2. The method of claim 1, wherein the reducing process is a dry process performed in a dry and vacuum chamber.

3. The method of claim 2, wherein a gas source of the plasma, used in the dry process, comprises hydrogen or hydrogen/nitrogen.

4. The method of claim 1, wherein the reducing process includes a thermal bake step in hydrogen or hydrogen/nitrogen.

5 The method of claim 4, wherein the thermal bake step is performed at a temperature from about 25 °C to about 200 °C.

6. The method of claim 4, wherein the substrate is exposed to an ultra-violet (UV) or electron beam (e-beam) during the thermal bake step.

7. The method of claim 1, wherein the exposed metal surface is oxidized before the reducing process is performed.

8. The method of claim 1, wherein the metal deposition is performed by an electrochemical

deposition process or displacement deposition process.

9. The method of claim 1, wherein the metal layer deposition is performed by electroless deposition

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10. The method of claim 1, wherein a metal activation step is performed before the metal layer deposition.

11. The method of claim 10, wherein the metal activation step is a self activation step.

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12. The method of claim 10, wherein the metal activation step is a palladium activation step.