

Abstract of the Disclosure

An operational margin of a memory of a semiconductor integrated circuit device including an SRAM is improved. In order to set the V_{th} of driving MISFETs Q_d , transfer MISFETs Q_t and MISFETs for load resistance Q_L forming memory cells of an SRAM, relatively and intentionally higher than the V_{th} of predetermined MISFETs of SRAM peripheral circuits and logic circuits such as microprocessor, an impurity introduction step is introduced to set the V_{th} of the driving MISFETs Q_d , transfer MISFETs Q_t and MISFETs for load resistance, separately from an impurity introduction step for setting the V_{th} of the predetermined MISFETs.

This Sheet Has Been Replaced

