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(71) Applicant: INTEL CORPORATION [US/US]; Mission College Boulevard, P.O. Box 58119, Santa Clara, CA 95052-8119 (US).

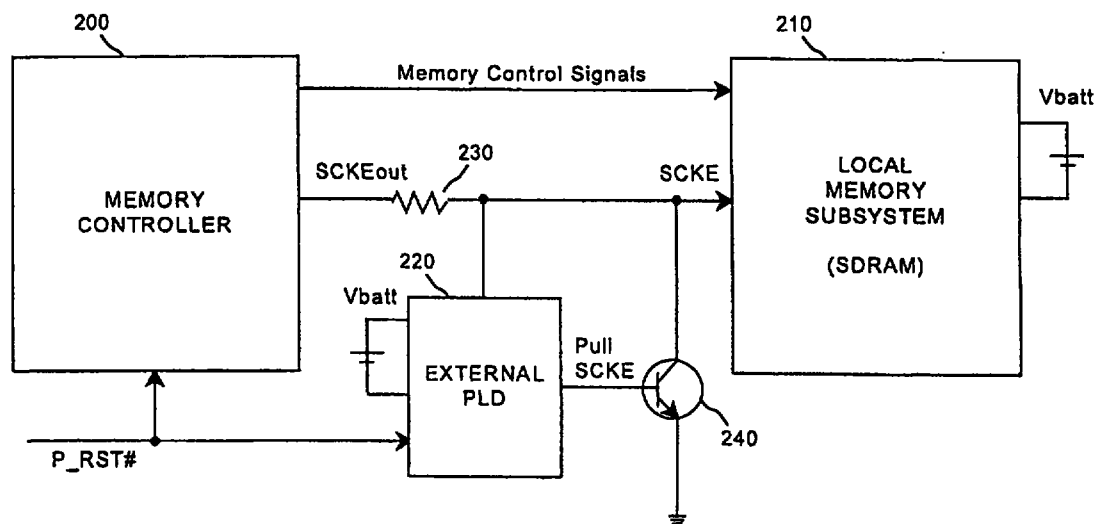
(72) Inventor: CRETA, Kenneth, C.; 3010 37th Street, N.W., Gig Harbor, WA 98335 (US).

(74) Agents: HELLER, Paul, H. et al.; Kenyon & Kenyon, Suite 700, 1500 K Street, N.W., Washington, DC 20005 (US).

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(54) Title: POWER FAILURE MODE FOR A MEMORY CONTROLLER



(57) Abstract

A power failure mode for a memory controller (200), such as a memory controller used in an input/output processor (100), which, when the memory controller has system power, refreshes a memory unit (210), such as an SDRAM memory unit, as required to maintain the memory image. In one embodiment, when a power failure occurs, the memory controller issues a self-refresh command to the memory, which has battery-backup power. A PCI reset signal may be used to determine when a power failure has occurred. The self-refresh command places the memory in a self-refresh mode, and a programmable logic device may be used to ensure that a clock enable signal input to the memory maintains the self-refresh mode. When system power returns, the memory controller resumes refreshing the memory.