FIG. 1

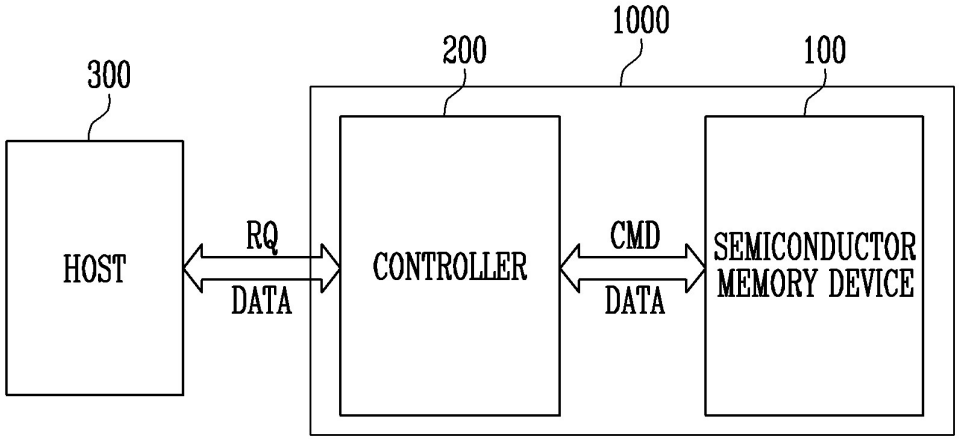

1000
200
100
300
HOST
RQ
DATA
CONTROLLER
CMD
DATA
SEMICONDUCTOR
MEMORY DEVICE

FIG. 2

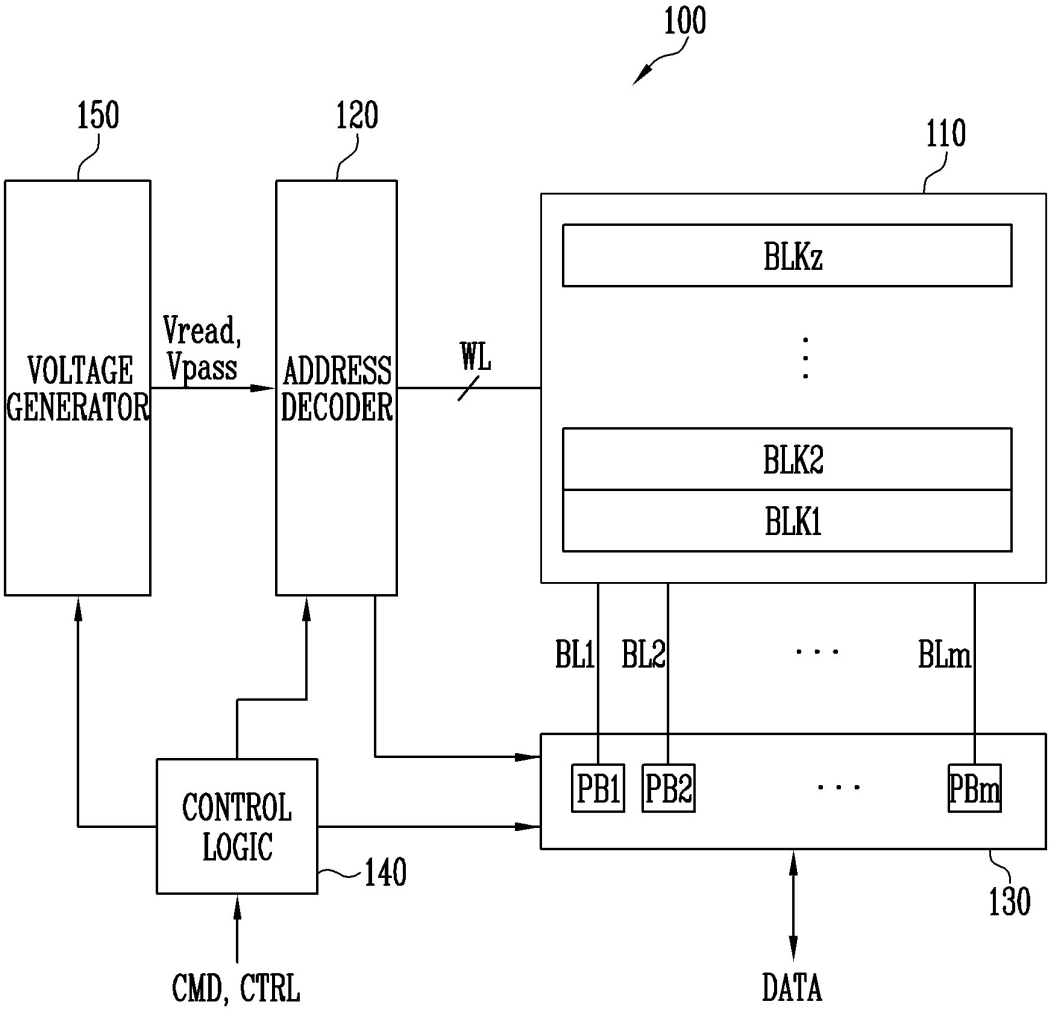

100
150
120
110
VOLTAGE GENERATOR
Vread, Vpass
ADDRESS DECODER
WL
BLKz
BLK2
BLK1
BL1
BL2
BLm
PB1
PB2
PBm
CONTROL LOGIC
140
130
CMD, CTRL
DATA

FIG. 3

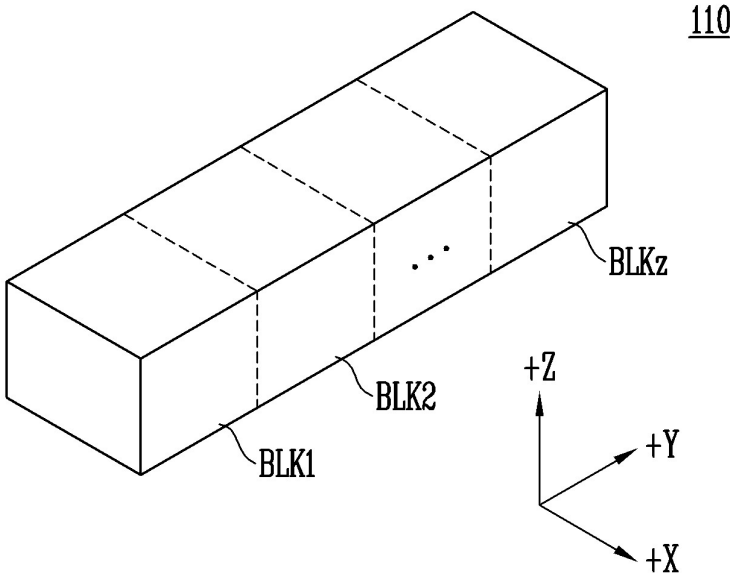


FIG. 4

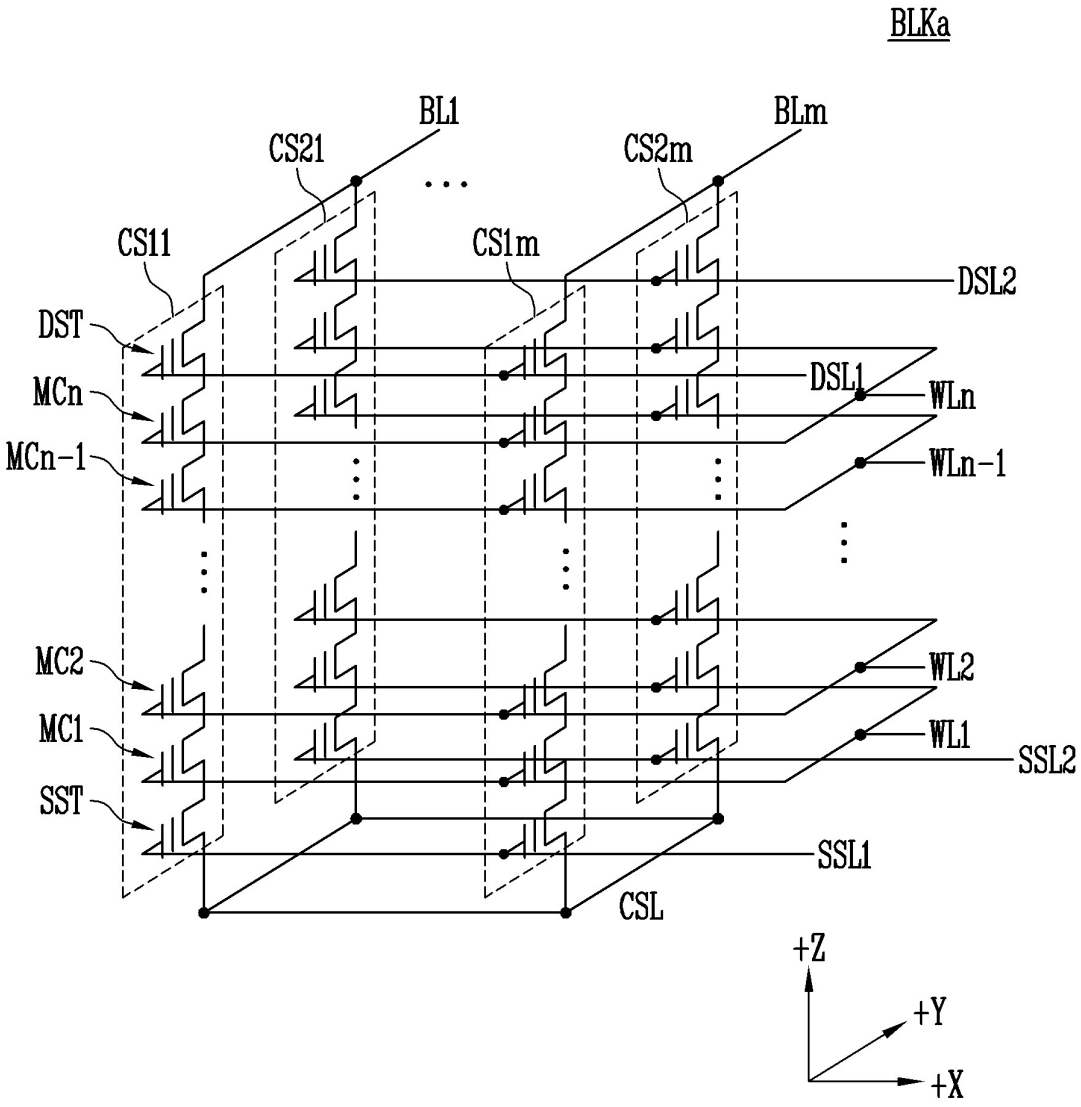

BLKa
BL1
BLm
CS21
CS2m
CS11
CS1m
DSL2
DST
DSL1
MCn
WLn
MCn-1
WLn-1
MC2
WL2
MC1
WL1
SSL2
SST
SSL1
CSL
+Z
+Y
+X

FIG. 5

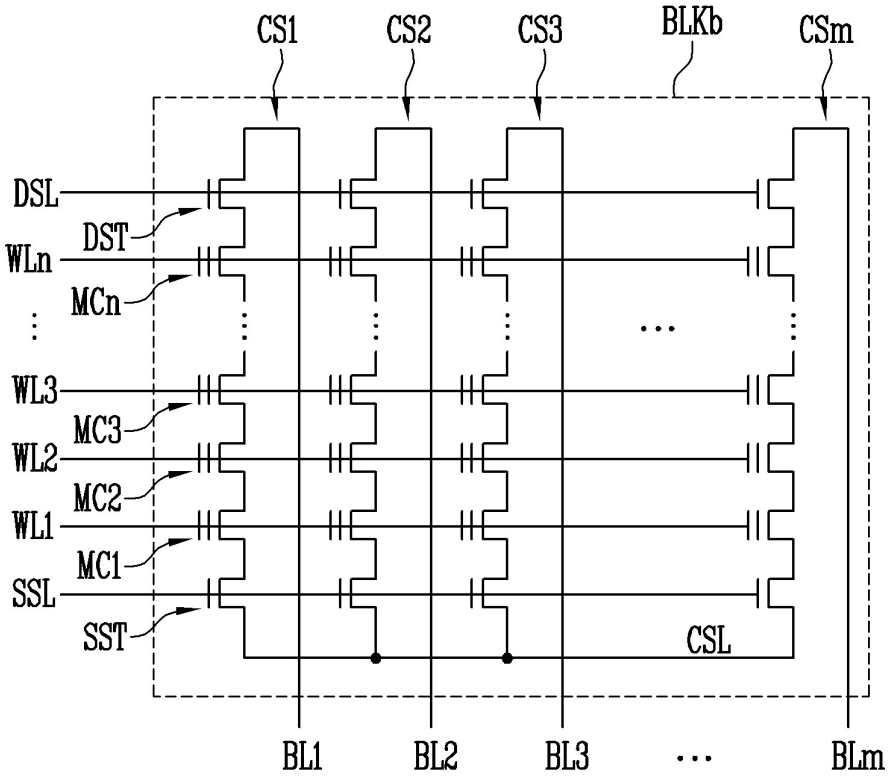

CS1
CS2
CS3
BLKb
CSm
DSL
DST
WLn
MCn
WL3
MC3
WL2
MC2
WL1
MC1
SSL
SST
CSL
BL1
BL2
BL3
BLm

FIG. 6

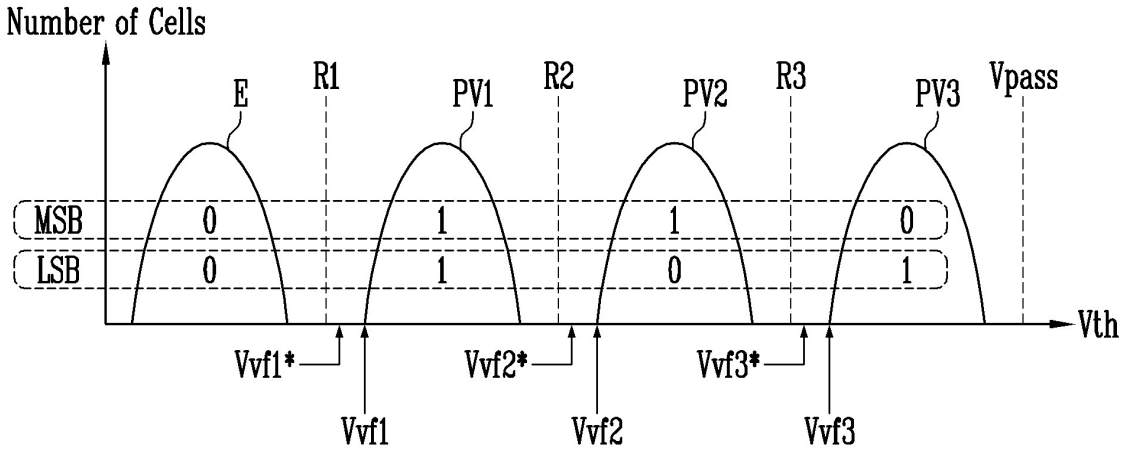

Number of Cells
E
R1
PV1
R2
PV2
R3
PV3
Vpass
MSB
LSB
0
1
1
0
0
1
0
1
Vth
Vvf1*
Vvf2*
Vvf3*
Vvf1
Vvf2
Vvf3

FIG. 7

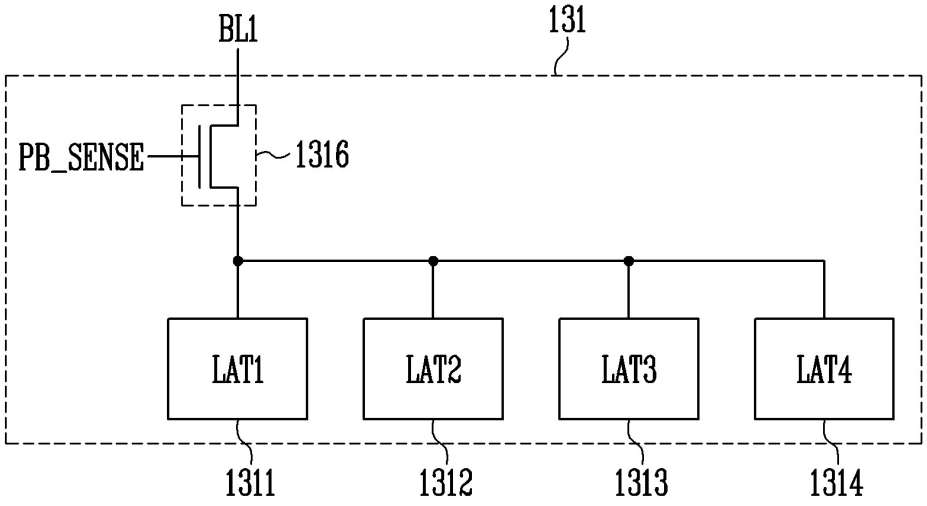

BL1
131
PB_SENSE
1316
LAT1
LAT2
LAT3
LAT4
1311
1312
1313
1314

FIG. 8A

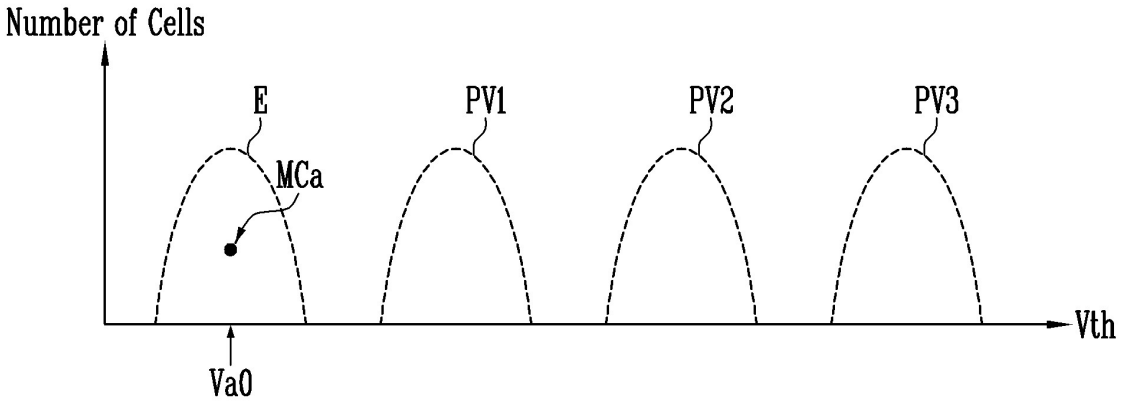


FIG. 8B

Vth	LAT1	LAT2	LAT3
Va0	0	0	X

FIG. 9A

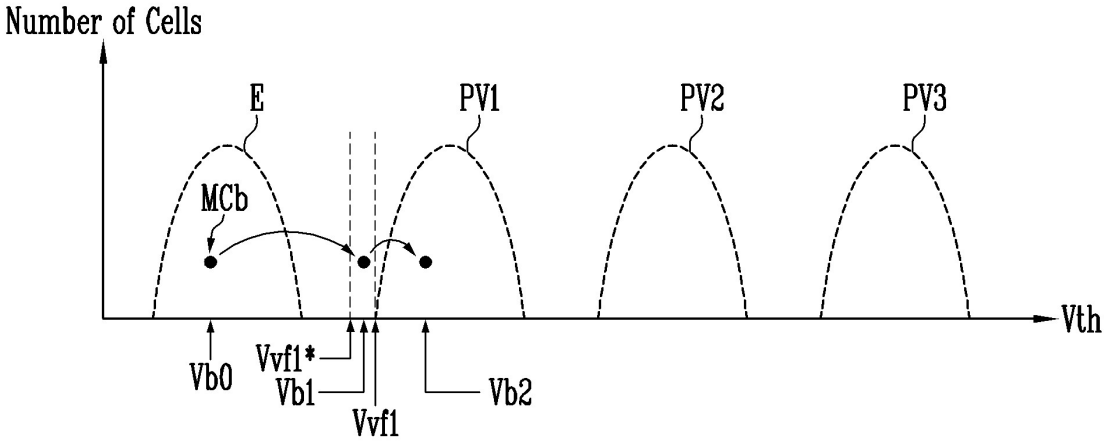


FIG. 9B

Vth	LAT1	LAT2	LAT3
Vb0	1	1	0
Vb1	1	1	1
Vb2	0	0	X

FIG. 10A

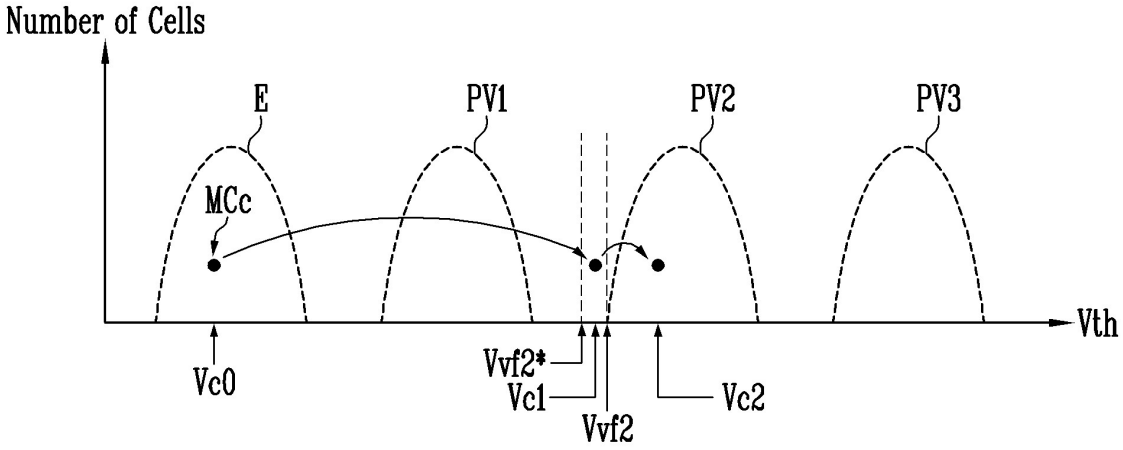


FIG. 10B

Vth	LAT1	LAT2	LAT3
Vc0	1	0	0
Vc1	1	0	1
Vc2	0	0	X

FIG. 11A

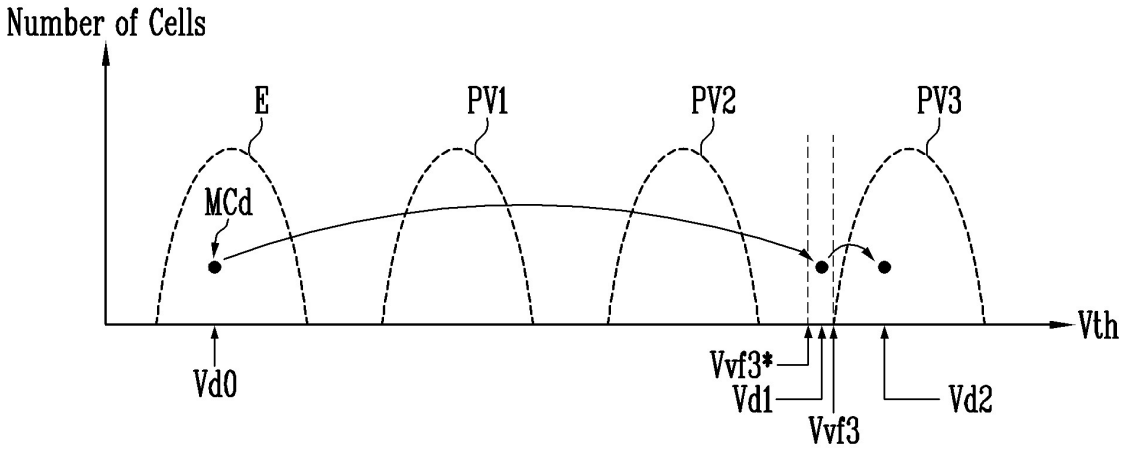


FIG. 11B

Vth	LAT1	LAT2	LAT3
Vd0	0	1	0
Vd1	0	1	1
Vd2	0	0	X

FIG. 12A

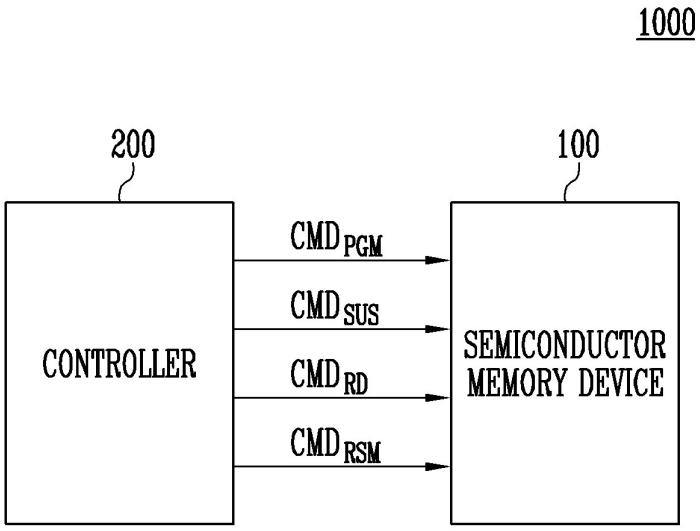


FIG. 12B

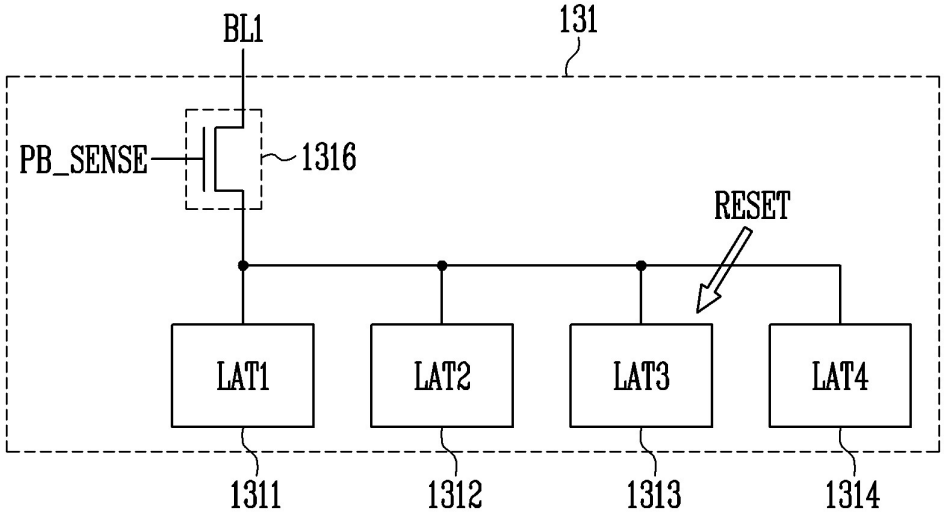


FIG. 13

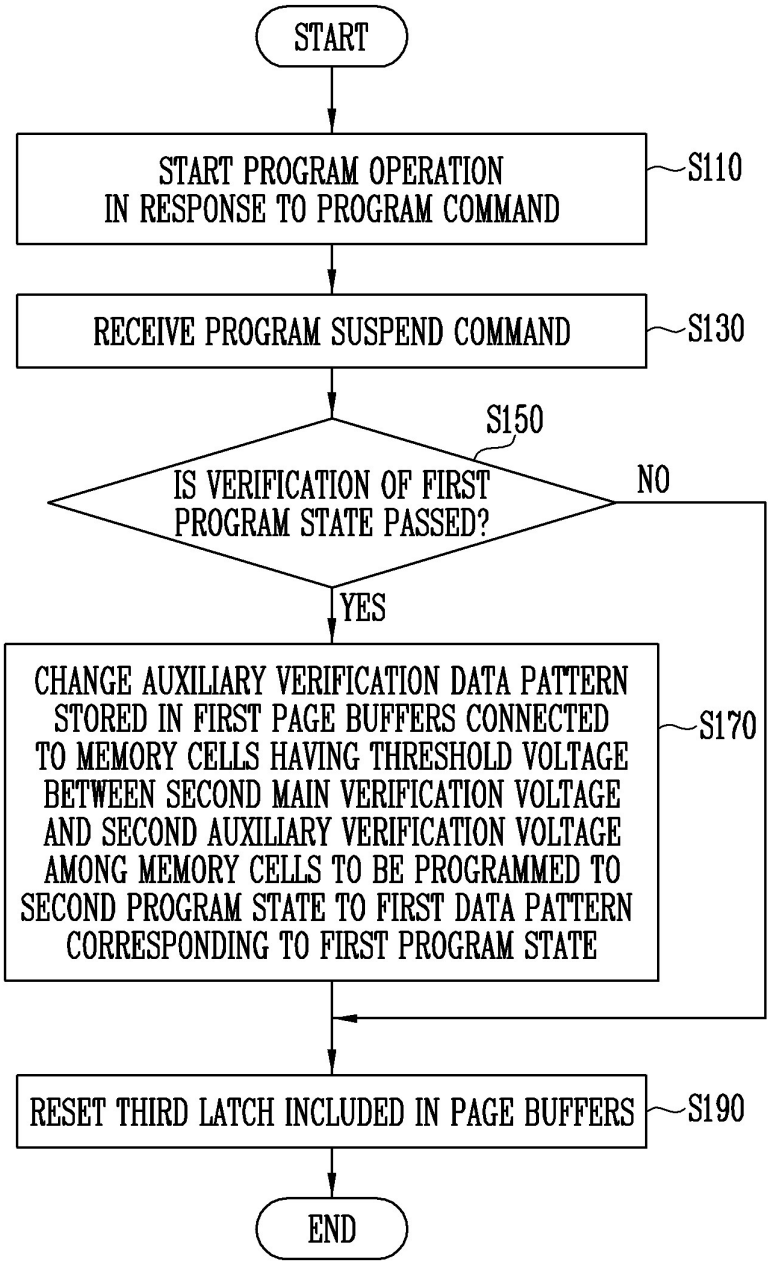

START
START PROGRAM OPERATION IN RESPONSE TO PROGRAM COMMAND
S110
RECEIVE PROGRAM SUSPEND COMMAND
S130
S150
IS VERIFICATION OF FIRST PROGRAM STATE PASSED?
NO
YES
CHANGE AUXILIARY VERIFICATION DATA PATTERN STORED IN FIRST PAGE BUFFERS CONNECTED TO MEMORY CELLS HAVING THRESHOLD VOLTAGE BETWEEN SECOND MAIN VERIFICATION VOLTAGE AND SECOND AUXILIARY VERIFICATION VOLTAGE AMONG MEMORY CELLS TO BE PROGRAMMED TO SECOND PROGRAM STATE TO FIRST DATA PATTERN CORRESPONDING TO FIRST PROGRAM STATE
S170
RESET THIRD LATCH INCLUDED IN PAGE BUFFERS
S190
END

FIG. 14A

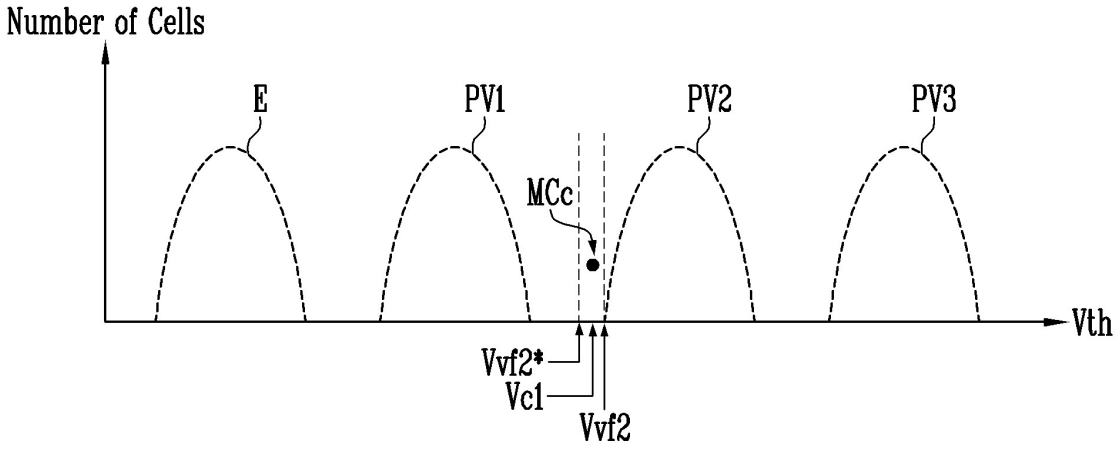


FIG. 14B

Vth	LAT1	LAT2	LAT3
Vc0	1	0	0
Vc1	1	0	1
Vc2	0	0	X

S170

Vth	LAT1	LAT2	LAT3
Vc0	1	0	0
Vc1	1	1	1
Vc2	0	0	X

FIG. 15

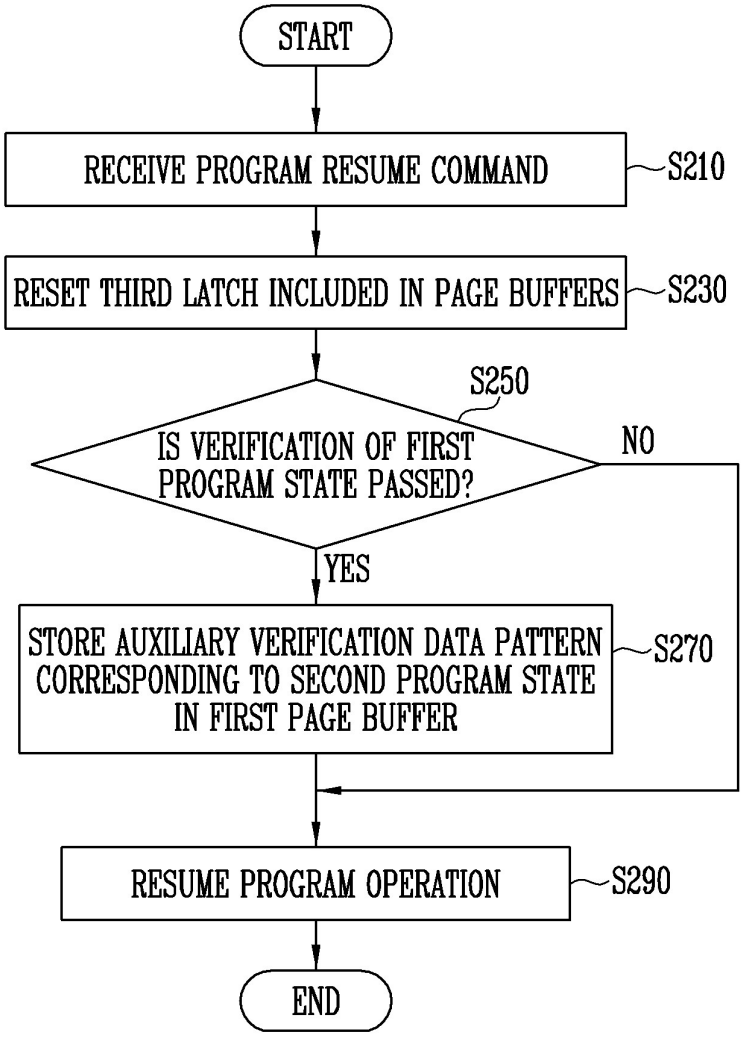

START
RECEIVE PROGRAM RESUME COMMAND
S210
RESET THIRD LATCH INCLUDED IN PAGE BUFFERS
S230
S250
IS VERIFICATION OF FIRST PROGRAM STATE PASSED?
NO
YES
STORE AUXILIARY VERIFICATION DATA PATTERN CORRESPONDING TO SECOND PROGRAM STATE IN FIRST PAGE BUFFER
S270
RESUME PROGRAM OPERATION
S290
END

FIG. 16

Vth	LAT1	LAT2	LAT3
Vc0	1	0	X
Vc1	1	1	X
Vc2	0	0	X

S230

Vth	LAT1	LAT2	LAT3
Vc0	1	0	0
Vc1	1	1	0
Vc2	0	0	0

S270

Vth	LAT1	LAT2	LAT3
Vc0	1	0	0
Vc1	1	0	1
Vc2	0	0	0

FIG. 17A

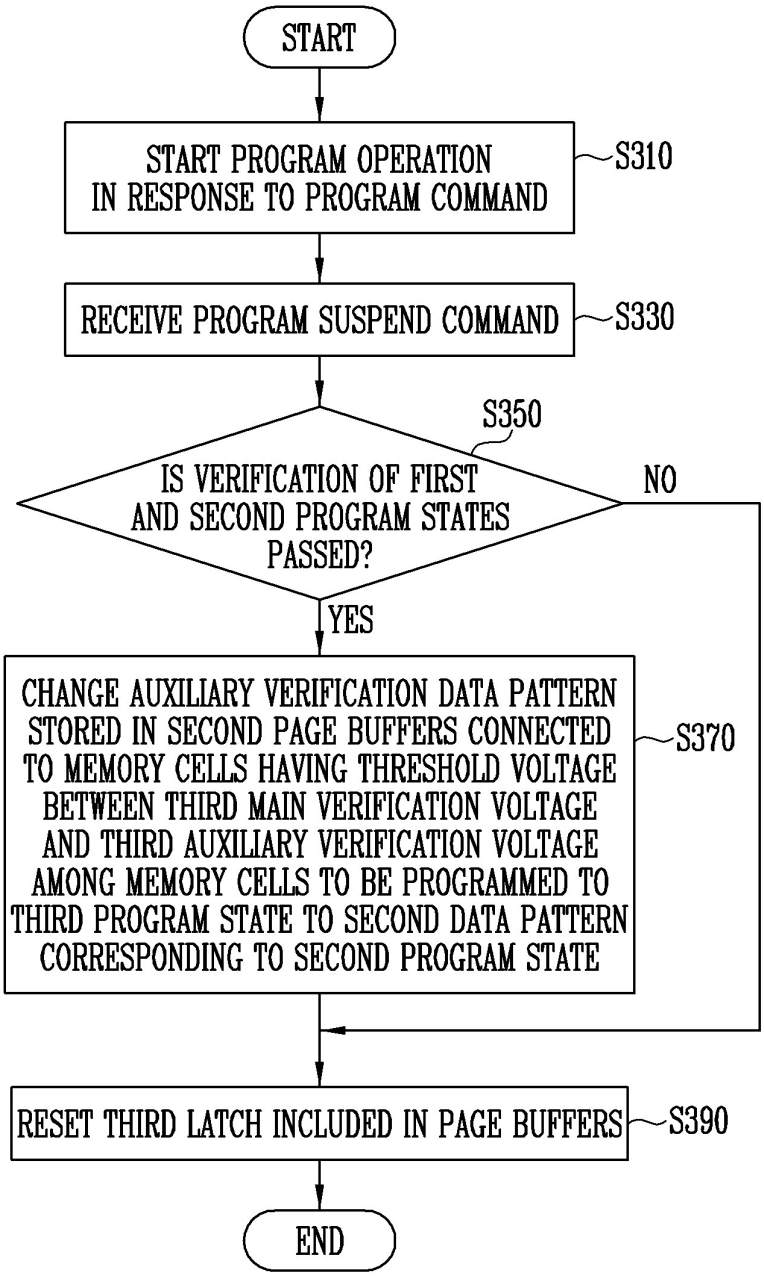

START
START PROGRAM OPERATION IN RESPONSE TO PROGRAM COMMAND
S310
RECEIVE PROGRAM SUSPEND COMMAND
S330
S350
IS VERIFICATION OF FIRST AND SECOND PROGRAM STATES PASSED?
NO
YES
CHANGE AUXILIARY VERIFICATION DATA PATTERN STORED IN SECOND PAGE BUFFERS CONNECTED TO MEMORY CELLS HAVING THRESHOLD VOLTAGE BETWEEN THIRD MAIN VERIFICATION VOLTAGE AND THIRD AUXILIARY VERIFICATION VOLTAGE AMONG MEMORY CELLS TO BE PROGRAMMED TO THIRD PROGRAM STATE TO SECOND DATA PATTERN CORRESPONDING TO SECOND PROGRAM STATE
S370
RESET THIRD LATCH INCLUDED IN PAGE BUFFERS
S390
END

FIG. 17B

Vth	LAT1	LAT2	LAT3
Vd0	0	1	0
Vd1	0	1	1
Vd2	0	0	X

S370

Vth	LAT1	LAT2	LAT3
Vd0	0	1	0
Vd1	1	0	1
Vd2	0	0	X

FIG. 18A

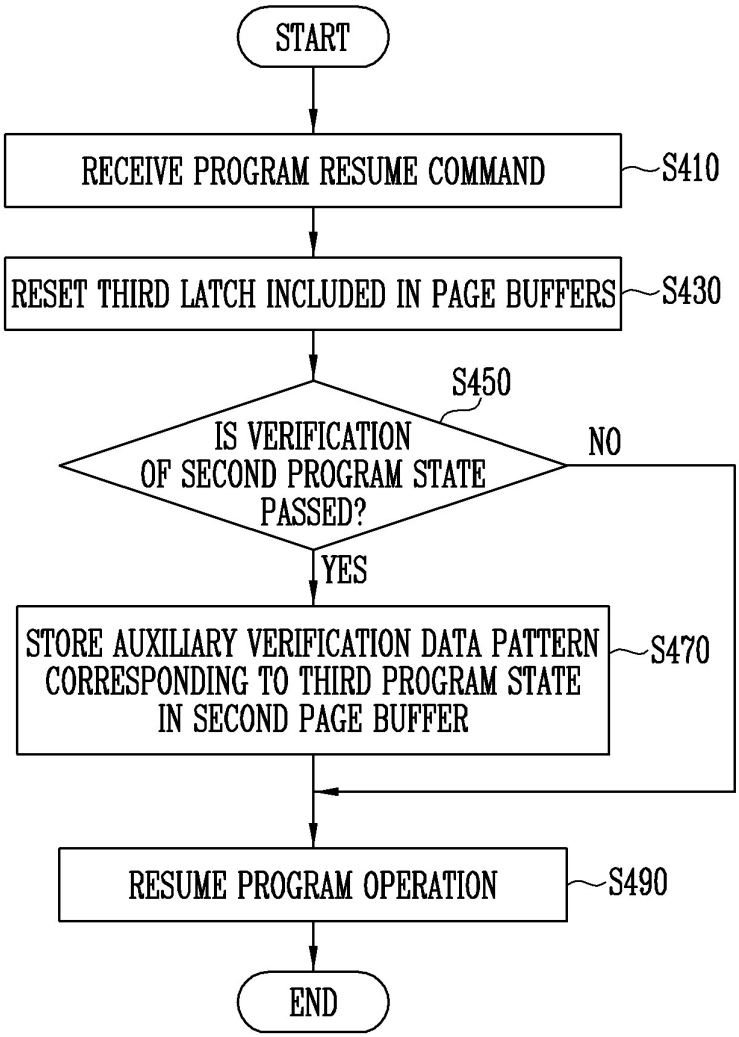

START
RECEIVE PROGRAM RESUME COMMAND
S410
RESET THIRD LATCH INCLUDED IN PAGE BUFFERS
S430
S450
IS VERIFICATION OF SECOND PROGRAM STATE PASSED?
NO
YES
STORE AUXILIARY VERIFICATION DATA PATTERN CORRESPONDING TO THIRD PROGRAM STATE IN SECOND PAGE BUFFER
S470
RESUME PROGRAM OPERATION
S490
END

FIG. 18B

Vth	LAT1	LAT2	LAT3
Vd0	0	1	X
Vd1	1	0	X
Vd2	0	0	X

S430

Vth	LAT1	LAT2	LAT3
Vd0	0	1	0
Vd1	1	0	0
Vd2	0	0	0

S470

Vth	LAT1	LAT2	LAT3
Vd0	0	1	0
Vd1	0	1	1
Vd2	0	0	0

FIG. 19

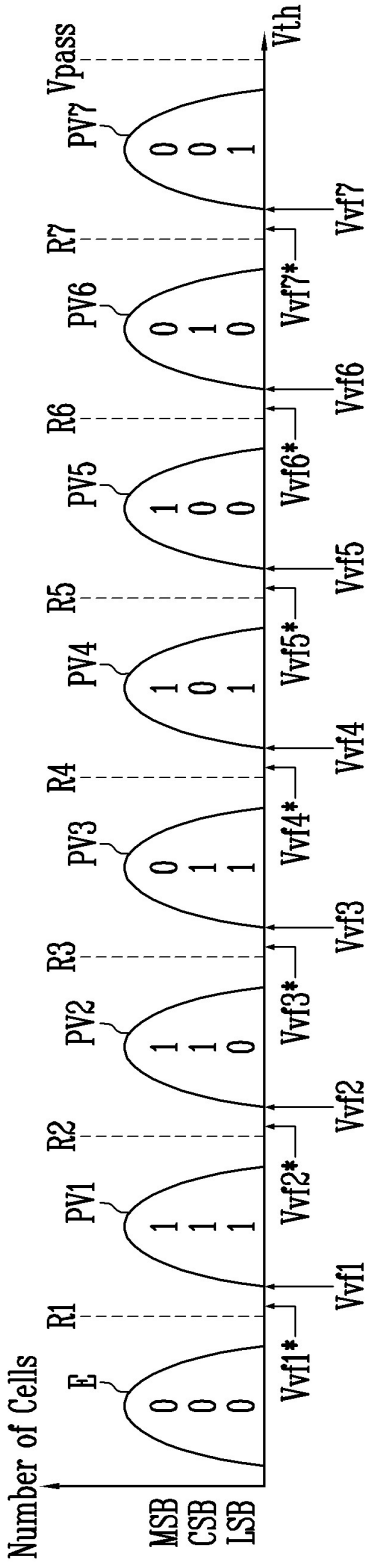

Number of Cells
Vth
MSB
CSB
LSB
E
PV1
PV2
PV3
PV4
PV5
PV6
PV7
R1
R2
R3
R4
R5
R6
R7
Vpass
Vvf1*
Vvf2*
Vvf3*
Vvf4*
Vvf5*
Vvf6*
Vvf7*
Vvf1
Vvf2
Vvf3
Vvf4
Vvf5
Vvf6
Vvf7
0 0 0
1 1 1
1 1 0
0 1 1
1 0 1
1 0 0
0 1 0
0 0 1

FIG. 20

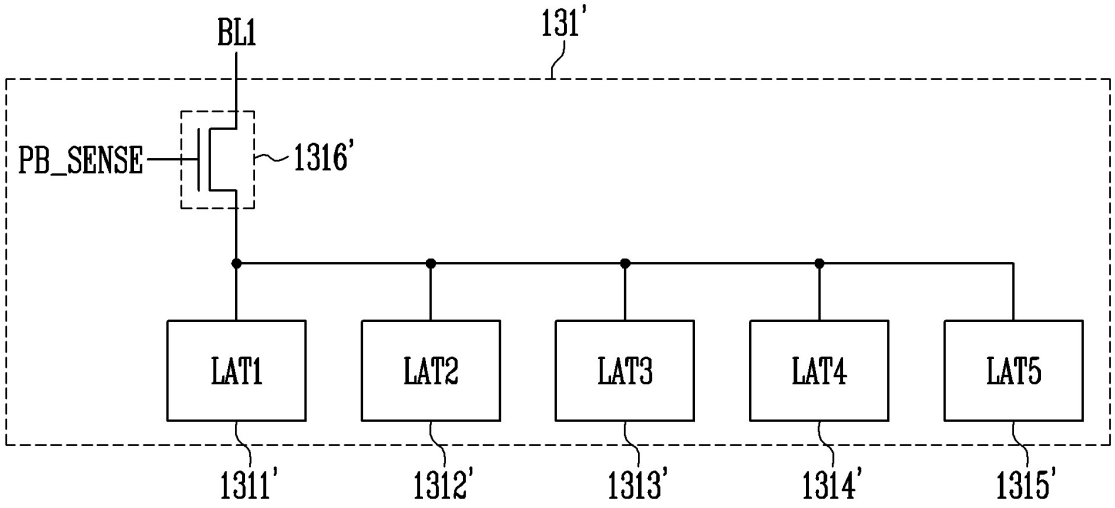

BL1
131'
PB_SENSE
1316'
LAT1
LAT2
LAT3
LAT4
LAT5
1311'
1312'
1313'
1314'
1315'

FIG. 21A

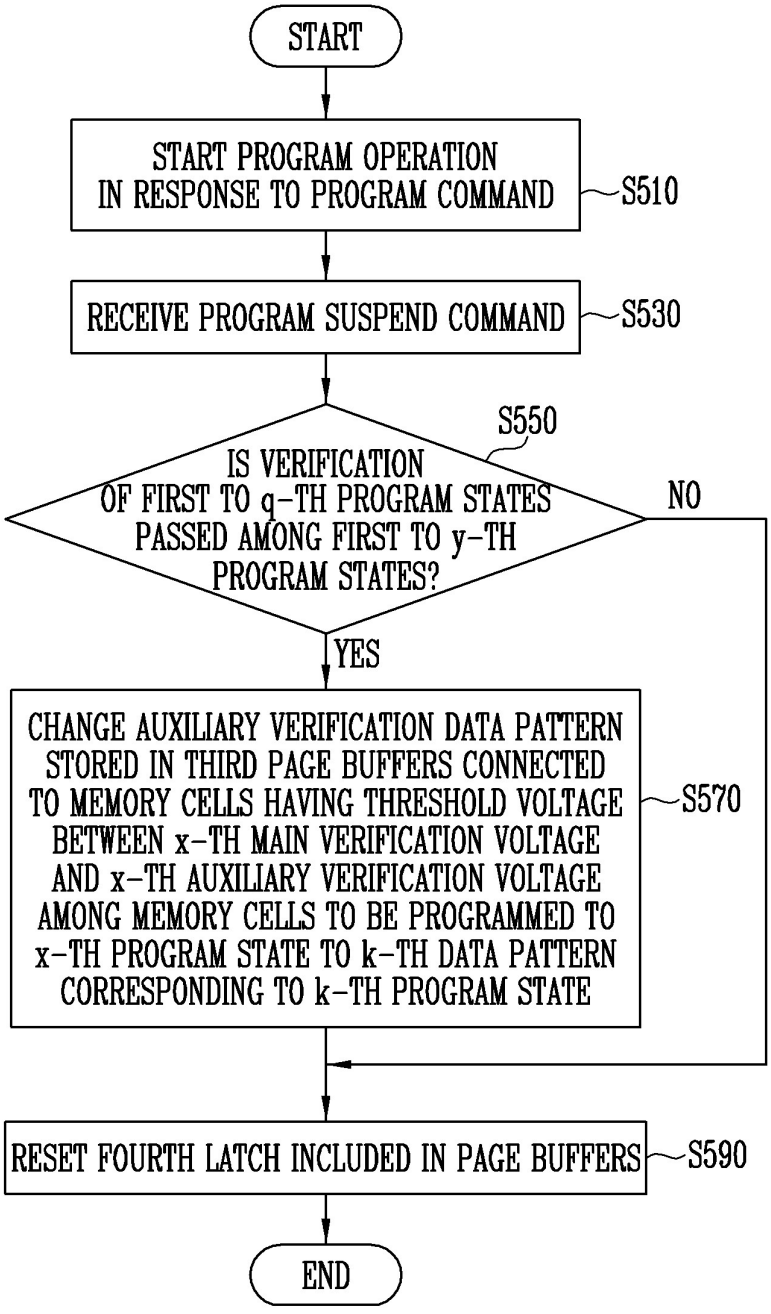

START
START PROGRAM OPERATION IN RESPONSE TO PROGRAM COMMAND
S510
RECEIVE PROGRAM SUSPEND COMMAND
S530
S550
IS VERIFICATION OF FIRST TO q-TH PROGRAM STATES PASSED AMONG FIRST TO y-TH PROGRAM STATES?
NO
YES
CHANGE AUXILIARY VERIFICATION DATA PATTERN STORED IN THIRD PAGE BUFFERS CONNECTED TO MEMORY CELLS HAVING THRESHOLD VOLTAGE BETWEEN x-TH MAIN VERIFICATION VOLTAGE AND x-TH AUXILIARY VERIFICATION VOLTAGE AMONG MEMORY CELLS TO BE PROGRAMMED TO x-TH PROGRAM STATE TO k-TH DATA PATTERN CORRESPONDING TO k-TH PROGRAM STATE
S570
RESET FOURTH LATCH INCLUDED IN PAGE BUFFERS
S590
END

FIG. 21B

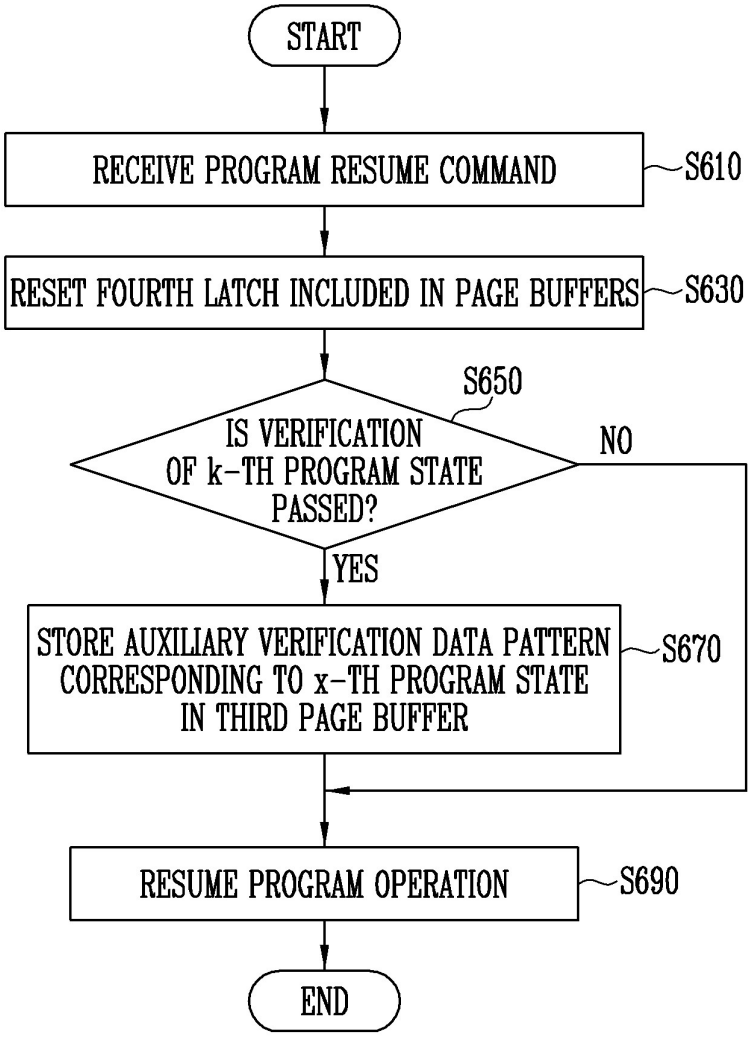

START
RECEIVE PROGRAM RESUME COMMAND
S610
RESET FOURTH LATCH INCLUDED IN PAGE BUFFERS
S630
S650
IS VERIFICATION OF k-TH PROGRAM STATE PASSED?
NO
YES
STORE AUXILIARY VERIFICATION DATA PATTERN CORRESPONDING TO x-TH PROGRAM STATE IN THIRD PAGE BUFFER
S670
RESUME PROGRAM OPERATION
S690
END

FIG. 22

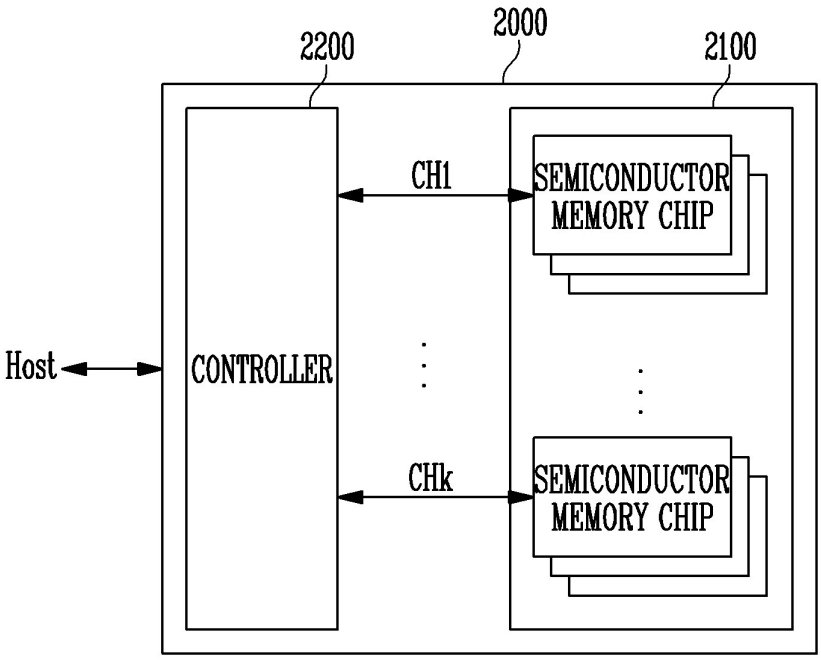
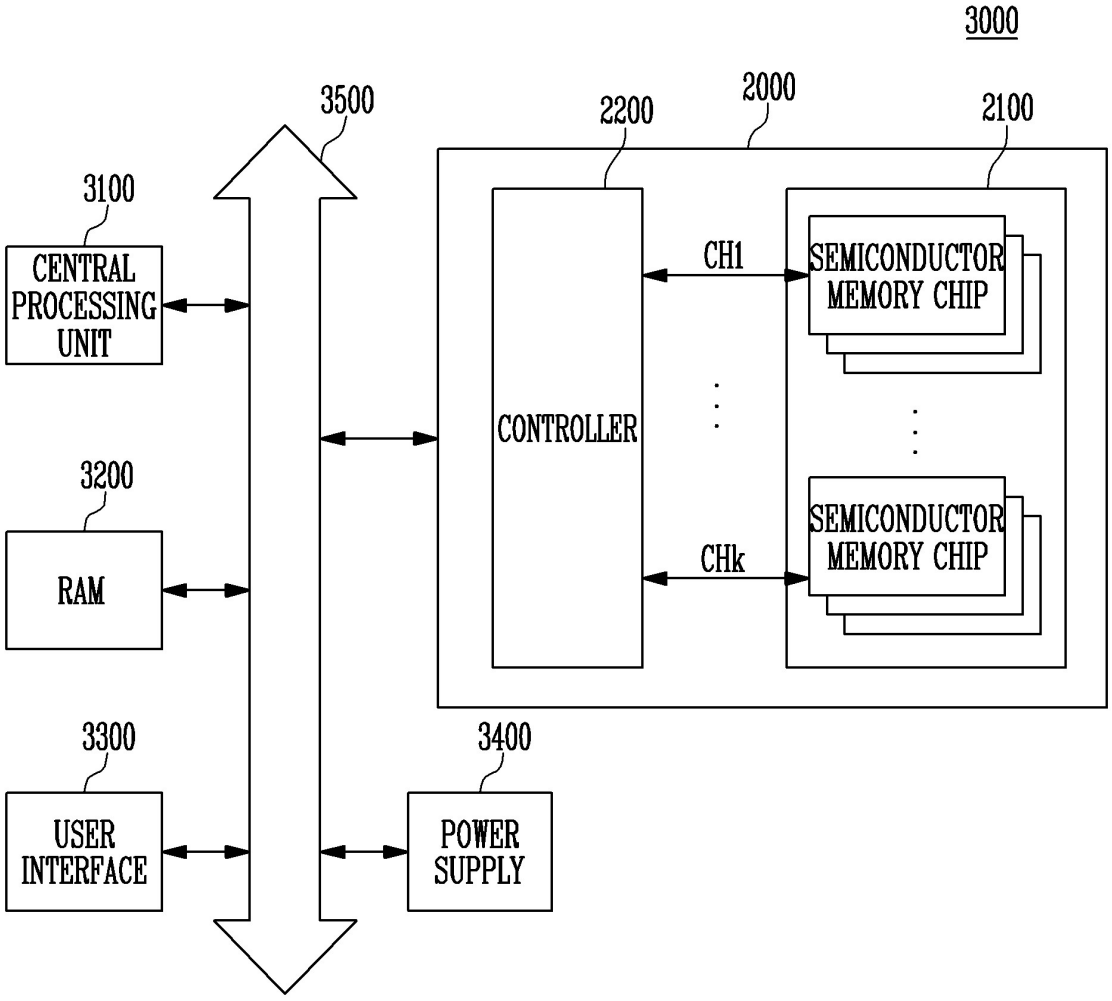

2200
2000
2100
CH1
SEMICONDUCTOR MEMORY CHIP
Host
CONTROLLER
CHk
SEMICONDUCTOR MEMORY CHIP

FIG. 23


3000
3500
2200
2000
2100
3100
CENTRAL PROCESSING UNIT
CH1
SEMICONDUCTOR MEMORY CHIP
CONTROLLER
3200
RAM
CHk
SEMICONDUCTOR MEMORY CHIP
3300
3400
USER INTERFACE
POWER SUPPLY