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(54) **Title:** BINARY ADDERS OF LOW TRANSISTOR COUNT

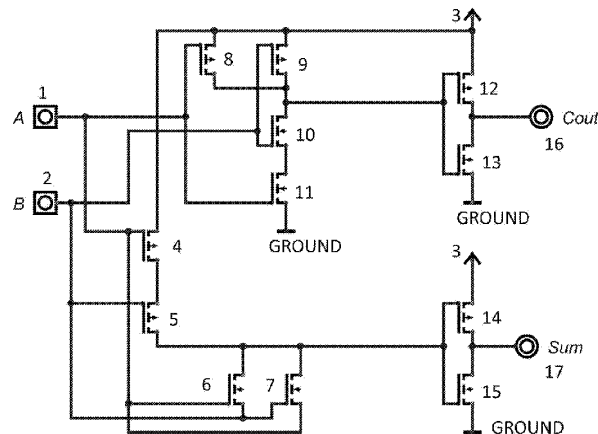


Fig. 1

(57) **Abstract:** A method for implementing a logic circuit employing a combination of binary adders of different lengths having summation and carry outputs and AND gates, comprising the steps of replacing at least one known CMOS implemented binary adder with an improved binary adder consisting of a logic block for performing summation between binary inputs of the logic block; a restoration block, connected between the output of the logic block and the output of the binary adder circuit, for compensating for voltage level losses when the output is in a high logic state or low logic state. The at least one CMOS AND gate is replaced with a high Fan-in AND gate being above a predetermined threshold, by an improved AND gate consisting of a logic block for performing an AND operation between binary inputs of the logic block; a restoration block, connected between the output of the logic block and the output of the AND gate, for compensating for voltage level losses when the output being in a high logic state or low logic state.

[Continued on next page]

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