WHAT IS CLAIMED IS:

1. A semiconductor chip, comprising:

a substrate;

an interlayer insulation layer including

a bottom interlayer insulation layer on an upper surface of the substrate, and

a top interlayer insulation layer on the bottom interlayer insulation layer;

an etch stop layer between the bottom interlayer insulation layer and the top interlayer insulation layer;

a landing pad on the interlayer insulation layer, the landing pad comprising a landing pad metal layer and a landing pad barrier layer, the landing pad barrier layer surrounding an upper surface of the landing pad metal layer and a side surface of the landing pad metal layer, the landing pad barrier layer being at least partially between the landing pad metal layer and the top interlayer insulation layer; and

a through via connected to the landing pad through the substrate, the interlayer insulation layer, and the etch stop layer,

wherein the etch stop layer is isolated from direct contact with the landing pad,

wherein the through via extends through a through via hole that exposes the landing pad barrier layer, the upper surface of the landing pad metal layer, and an inner sidewall of the landing pad metal layer, the through via extends through the landing pad barrier layer and directly contacts the landing pad metal layer, and a sidewall of the through via directly contacts the inner sidewall of the landing pad metal layer.

2. The semiconductor chip of claim 1, further comprising:

a via insulation layer surrounding a limited portion of the sidewall of the through via,

wherein the via insulation layer directly contacts the etch stop layer and does not directly contact the landing pad.

3. The semiconductor chip of claim 2, wherein the sidewall of the through via directly contacts the via insulation layer, the etch stop layer, the top interlayer insulation layer, and the landing pad.

4. The semiconductor chip of claim 2 or claim 3, wherein

a lower surface of the etch stop layer facing the upper surface of the substrate directly contacts the via insulation layer and the bottom interlayer insulation layer, and

an upper surface of the etch stop layer opposite to the upper surface of the substrate directly contacts the top interlayer insulation layer and does not directly contact the via insulation layer and the landing pad.

5. The semiconductor chip of claim 4, wherein

one sidewall of the via insulation layer directly contacts the through via,

another sidewall of the via insulation layer directly contacts the substrate and the bottom interlayer insulation layer, and

an upper surface of the via insulation layer opposite to the upper surface of the substrate directly contacts the lower surface of the etch stop layer.

6. The semiconductor chip of any one of claims 1 to 5, wherein a material of the etch stop layer has an etch selectivity with respect to a material of the bottom interlayer insulation layer.

7. The semiconductor chip of any one of claims 1 to 6, wherein

a thickness of the bottom interlayer insulation layer is greater than a thickness of the etch stop layer, and

the thickness of the etch stop layer is substantially equal to or greater than a thickness of the top interlayer insulation layer.

8. The semiconductor chip of any one of claims 1 to 7, wherein

at least a portion of the through via has a cross-section width which is progressively narrowed in proportion to distance of the cross-section of the portion of the through via from a bottom surface of the substrate in a direction extending along a longitudinal axis of the through via away from the bottom surface of the substrate, and

the landing pad has a cross-section width which is progressively widened in proportion to distance of the cross-section of the landing pad from the bottom surface of the substrate in the direction extending along the longitudinal axis of the through via away from the bottom surface of the substrate.

9. The semiconductor chip of any one of claims 1 to 8, wherein a material composition of the bottom interlayer insulation layer is different from a material composition of the top interlayer insulation layer.

10. The semiconductor chip of any one of claims 1 to 9, wherein the etch stop layer includes a stack of a plurality of different material layers.

11. A semiconductor chip, comprising:

a substrate;

an interlayer insulation layer on an upper surface of the substrate, the interlayer insulation layer surrounding a semiconductor device;

an inter-metal insulation layer surrounding a metal wiring and including

a bottom inter-metal insulation layer on the interlayer insulation layer, and

a top inter-metal insulation layer on the bottom inter-metal insulation layer;

an etch stop layer between the bottom inter-metal insulation layer and the top inter-metal insulation layer;

a landing pad on the inter-metal insulation layer, the landing pad comprising a landing pad metal layer and a landing pad barrier layer, the landing pad barrier layer surrounding an upper surface of the landing pad metal layer and a side surface of the landing pad metal layer, the landing pad barrier layer being at least partially between the landing pad metal layer and the top inter-metal insulation layer;

a bump structure on the landing pad; and

a through via connected to the landing pad through the substrate, the interlayer insulation layer, the inter-metal insulation layer, and the etch stop layer,

wherein the etch stop layer is isolated from direct contact with the landing pad,

wherein the through via extends through a through via hole that exposes the landing pad barrier layer, the upper surface of the landing pad metal layer, and an inner sidewall of the landing pad metal layer, the through via extends through the landing pad barrier layer and directly contacts the landing pad metal layer, and a sidewall of the through via directly contacts the inner sidewall of the landing pad metal layer.

12. The semiconductor chip of claim 11, further comprising:

a via insulation layer surrounding a limited portion of the sidewall of the through via, wherein

the via insulation layer directly contacts the substrate, the interlayer insulation layer, the bottom inter-metal insulation layer, and the etch stop layer, and

the via insulation layer does not directly contact the top inter-metal insulation layer and the landing pad.

13. The semiconductor chip of claim 12, wherein

a lower surface of the etch stop layer facing the upper surface of the substrate directly contacts the via insulation layer and the bottom inter-metal insulation layer, and

an upper surface of the etch stop layer opposite to the upper surface of the substrate directly contacts the top inter-metal insulation layer and does not directly contact the via insulation layer and the landing pad.

14. The semiconductor chip of any one of claims 11 to 13, further comprising:

a front-end-of-line (FEOL) structure on the upper surface of the substrate; and

a back-end-of-line (BEOL) structure on the FEOL structure,

wherein

the interlayer insulation layer is a portion of the FEOL structure, and

each of the metal wiring and the inter-metal insulation layer is a portion of the BEOL structure.

15. The semiconductor chip of claim 14, wherein

the etch stop layer is a portion of the BEOL structure, and

a portion of the metal wiring extends through the etch stop layer and directly contacts the landing pad.

16. A method of manufacturing a semiconductor chip, the method comprising:

forming a semiconductor device on a first surface of a substrate;

forming a bottom interlayer insulation layer on the first surface of the substrate, such that the bottom interlayer insulation layer surrounds the semiconductor device;

forming an etch stop layer on the bottom interlayer insulation layer;

forming a top interlayer insulation layer on the etch stop layer;

forming a landing pad on the top interlayer insulation layer, such that the landing pad is isolated from direct contact with the etch stop layer, the landing pad comprising a landing pad metal layer and a landing pad barrier layer, the landing pad barrier layer surrounding an upper surface of the landing pad metal layer and a side surface of the landing pad metal layer, the landing pad barrier layer being at least partially between the landing pad metal layer and the top interlayer insulation layer;

forming a preliminary through via hole that extends through the substrate, from a second surface of the substrate that is opposite to the first surface of the substrate, to expose the etch stop layer;

forming a via insulation layer on an inner wall of the preliminary through via hole to define a through via hole;

enlarging a floor of the through via hole to expose the landing pad barrier layer, the upper surface of the landing pad metal layer, and an inner sidewall of the landing pad metal layer; and

forming a through via filling the through via hole, such that the through via extends through the landing pad barrier layer and directly contacts the landing pad metal layer, and a sidewall of the through via directly contacts the inner sidewall of the landing pad metal layer.

17. The method of claim 16, wherein the forming the via insulation layer includes conformally forming the via insulation layer on a sidewall of the substrate, a sidewall of the bottom interlayer insulation layer, and an exposed surface of the etch stop layer.

18. The method of claim 16 or claim 17, wherein the enlarging of the floor of the through via hole includes

etching an exposed surface of the via insulation layer to expose the etch stop layer;

etching an exposed surface of the etch stop layer to expose the top interlayer insulation layer; and

etching an exposed surface of the top interlayer insulation layer to expose the upper surface of the landing pad metal layer.

19. The method of claim 18, wherein a material of the etch stop layer has an etch selectivity with respect to a material of the bottom interlayer insulation layer.

20. The method of any one of claims 16 to 19, wherein the forming the preliminary through via hole causes a height of a center portion of an exposed surface of the etch stop layer to be greater than a height of a peripheral portion of the exposed surface of the etch stop layer.