METHOD FOR REDUCING SILICIDE DEFECTS IN INTEGRATED CIRCUITS

ABSTRACT

A method for forming silicide contacts in integrated circuits (ICs) is described. A spacer pull-back etch is performed during the salicidation process to reduce the stress between the spacer and source/drain silicide contact at the spacer undercut. This prevents the propagation of surface defects into the substrate, thereby minimizing the occurrence of silicide pipe defects. The spacer pull-back etch can be performed after a first annealing step to form the silicide contacts.

Fig. 2