

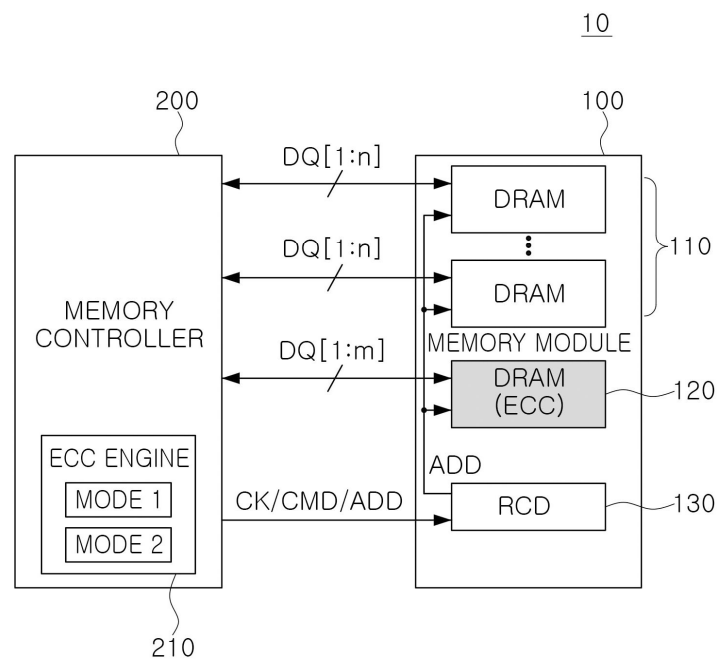


FIG. 1

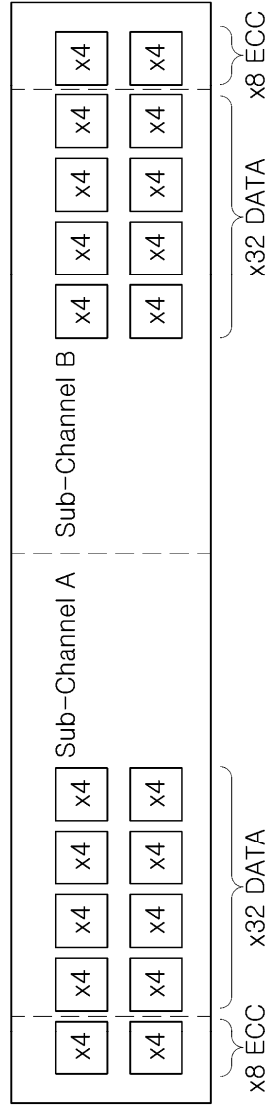


FIG. 2A

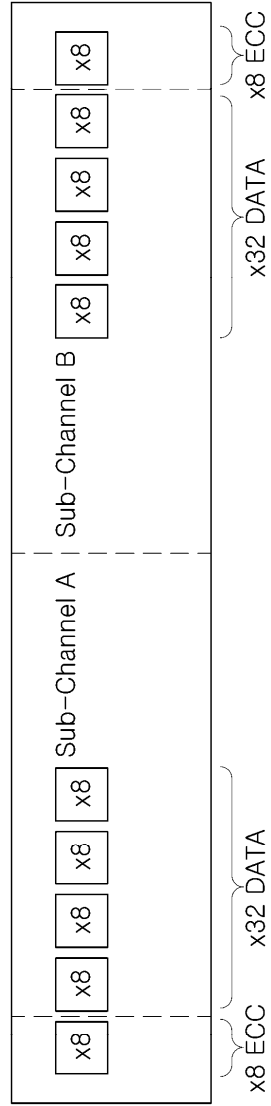


FIG. 2B

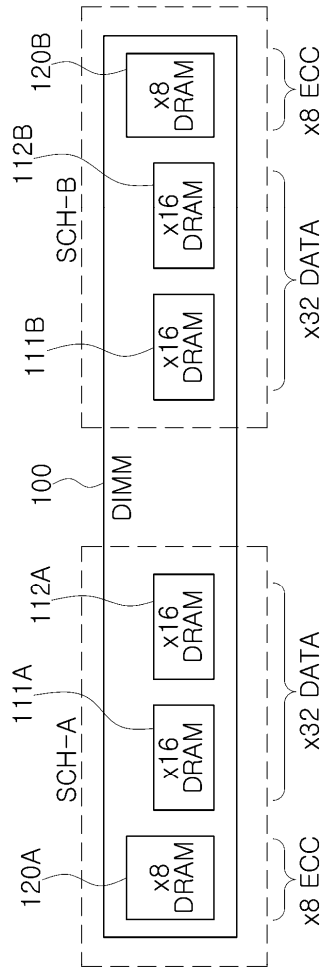


FIG. 3

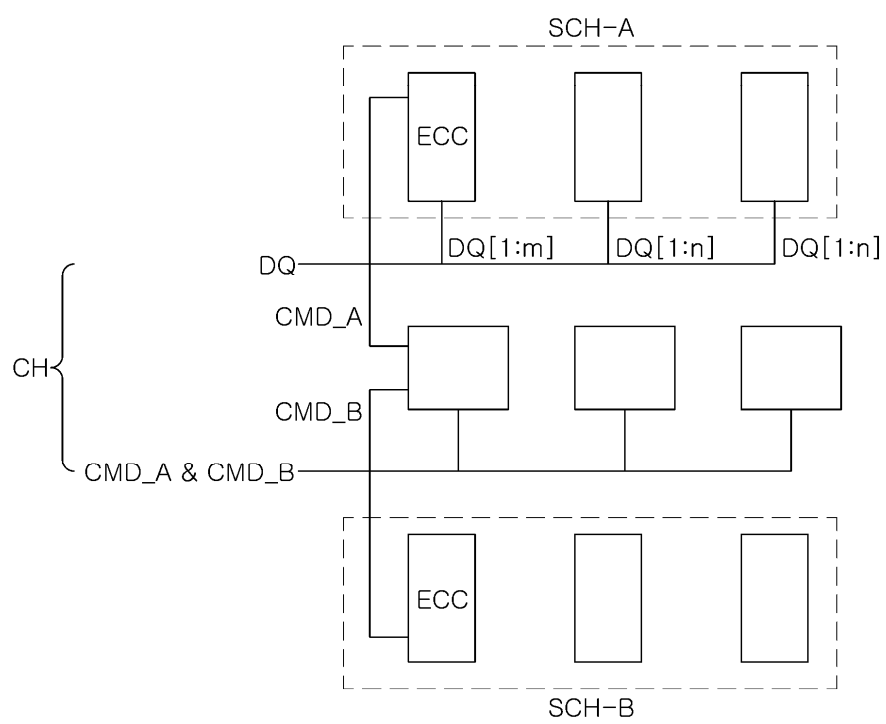


FIG. 4

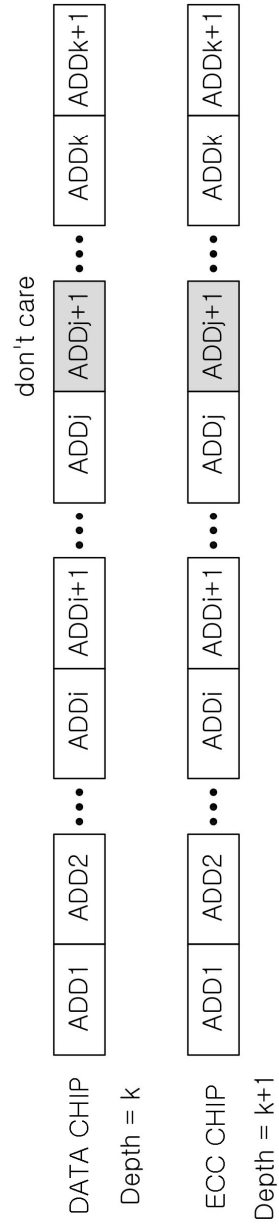


FIG. 5A

Configuration		4 Gb x4	2 Gb x8	1 Gb x8
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	#BG/ #Banks per BG/ # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDS / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

FIG. 5B

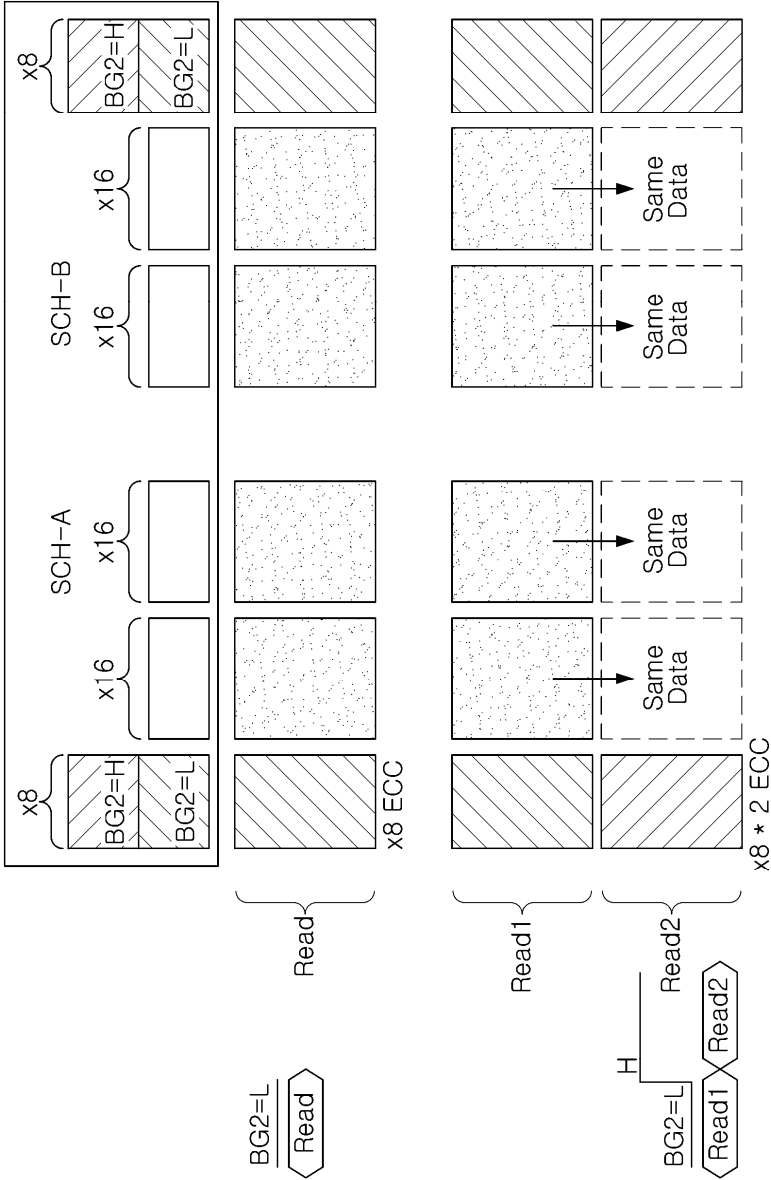


FIG. 6

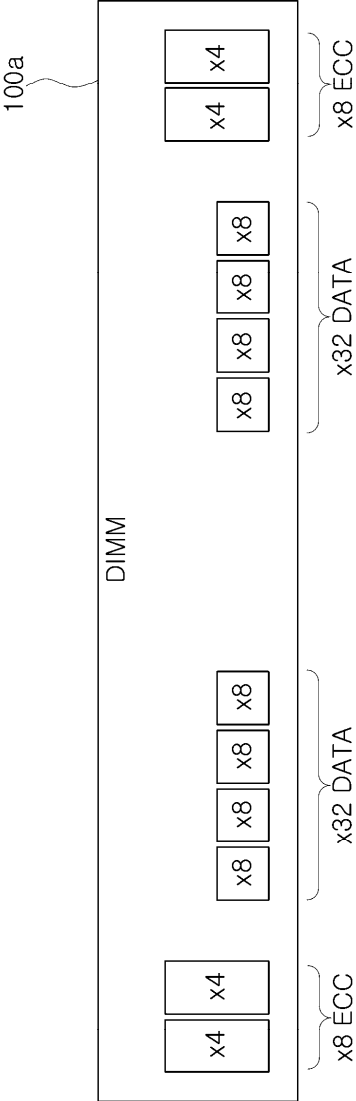


FIG. 7

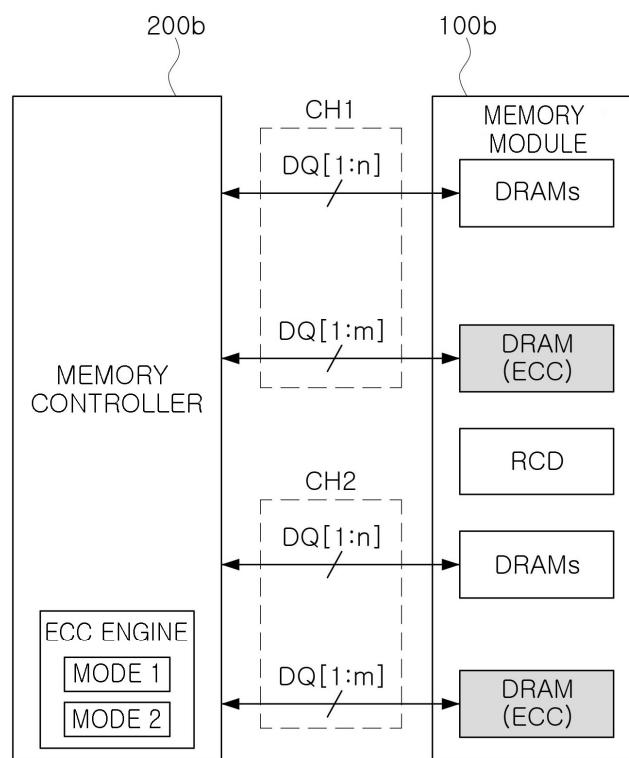


FIG. 8

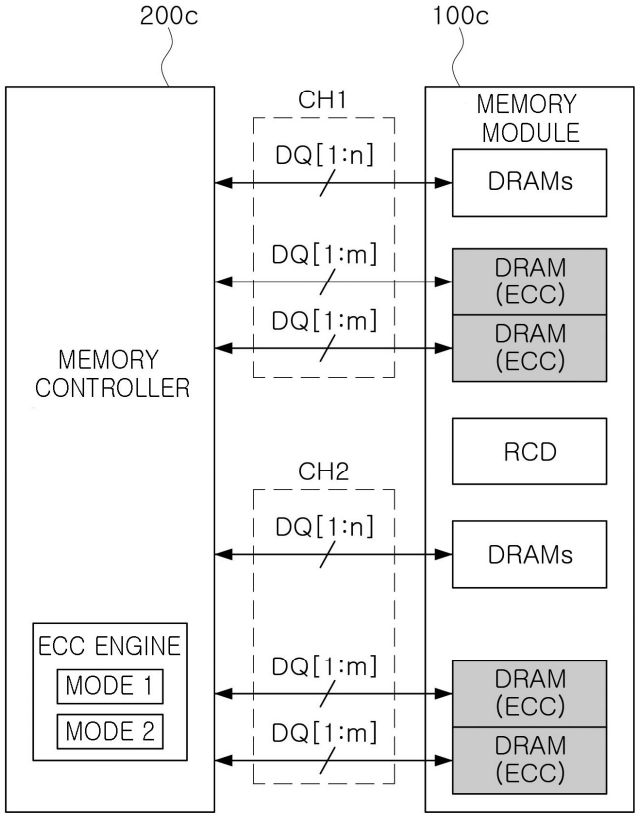


FIG. 9

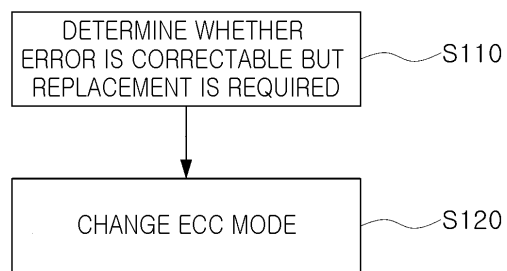


FIG. 10

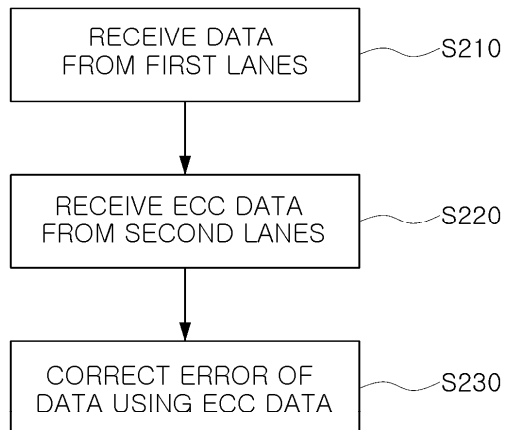


FIG. 11

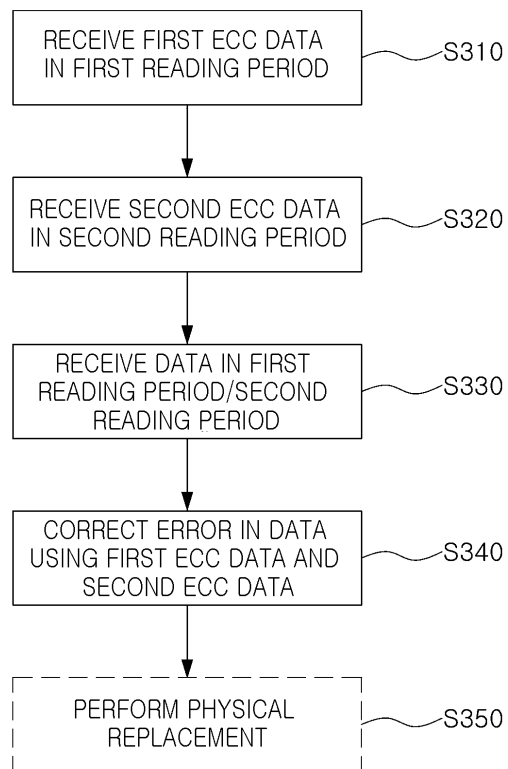


FIG. 12

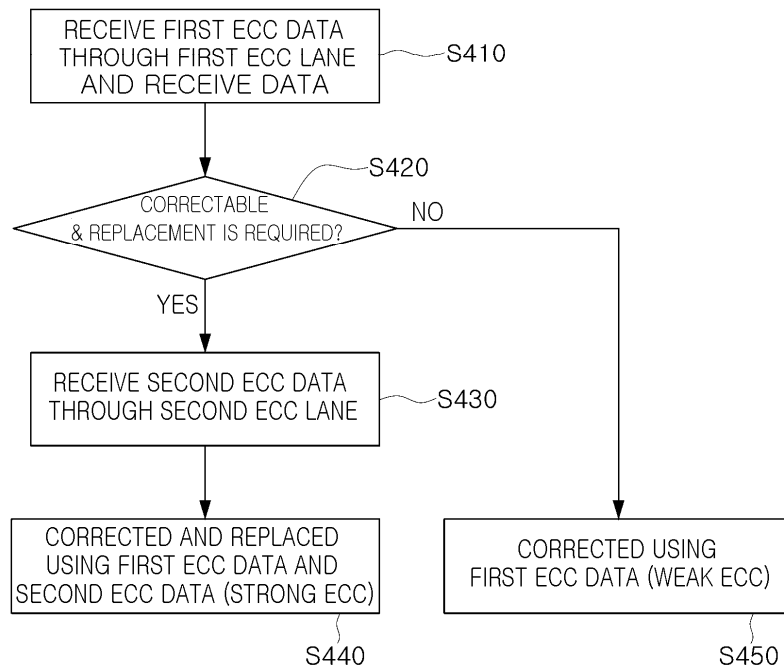


FIG. 13

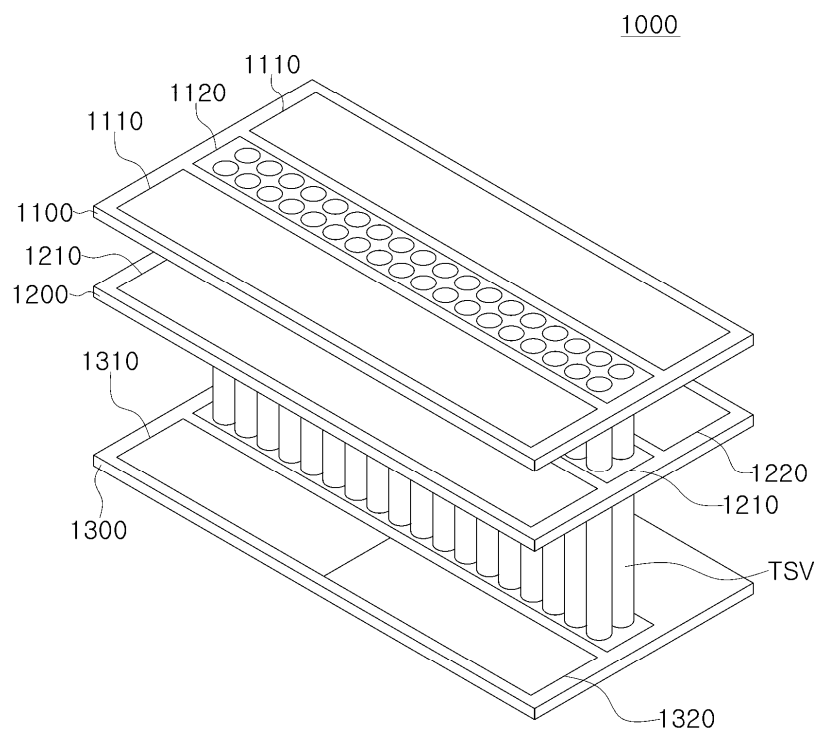


FIG. 14

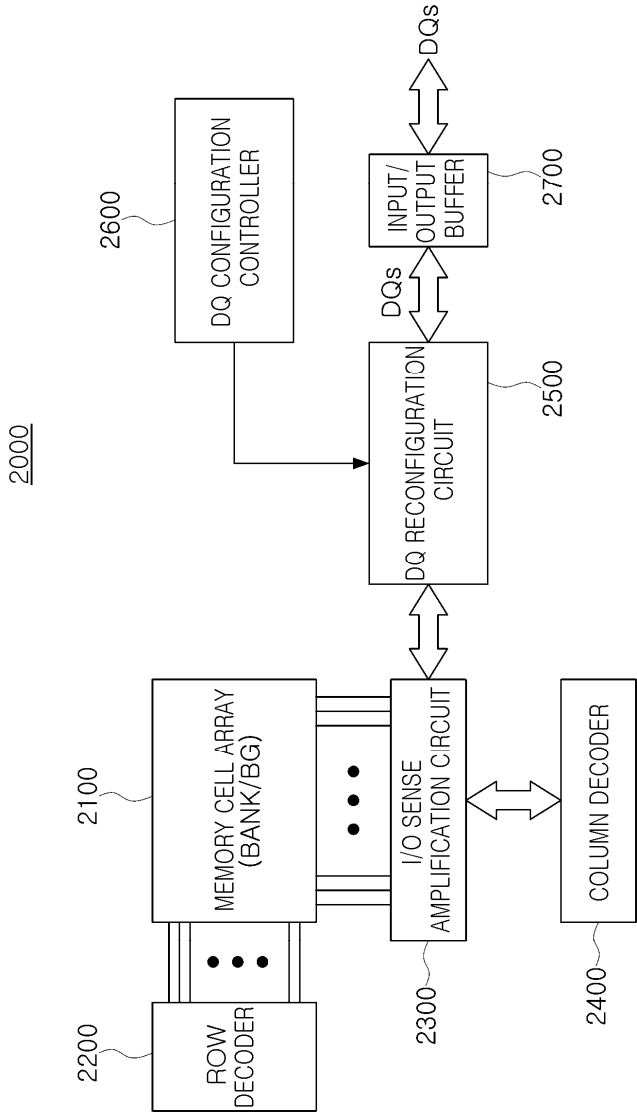


FIG. 15

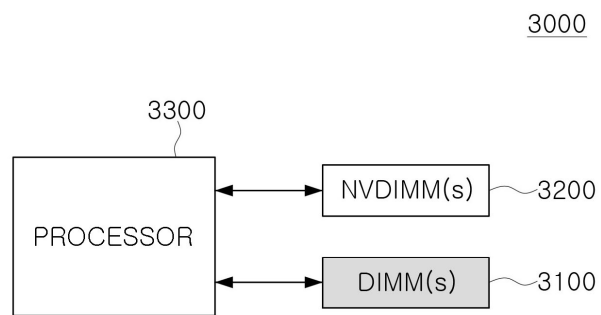


FIG. 16

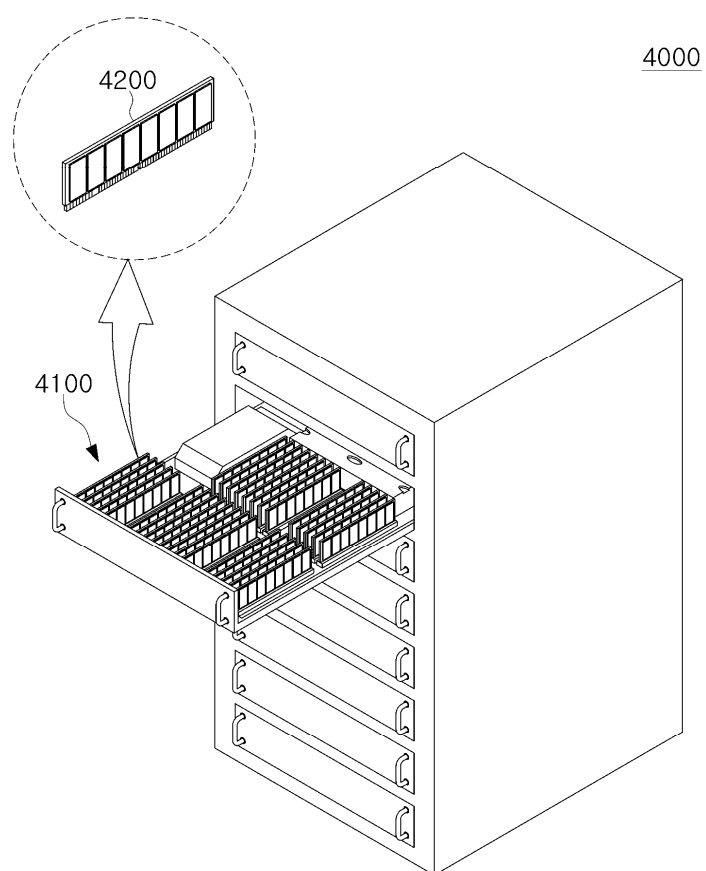


FIG. 17