Abstract

A video display unit and deflection system are synchronized with a first video signal. The video display unit may have a wide format display ratio. A detecting circuit (820) determines whether the first video signal has more than one field type (U/L). A second video signal has more than one field type. A multiplexer combines the first and a second video signals for a simultaneous video display. A video signal processor is responsive to the detecting circuit (820) and has two modes of operation. In a first mode of operation, when the first video signal has more than one field type, all fields of the second video signal are an output to the multiplexer. In a second mode of operation, when the first video signal has only one field type, only one field type of the second video signal is an output to the multiplexer. The video signal processor has a memory for storing the second video signal. Only one field type of the video signal is written into and read from the memory during the second mode of operation. Each field written into the memory during the second mode of operation is read out twice to the multiplexer.

FIGURE 14

This Sheet Has Been Replaced