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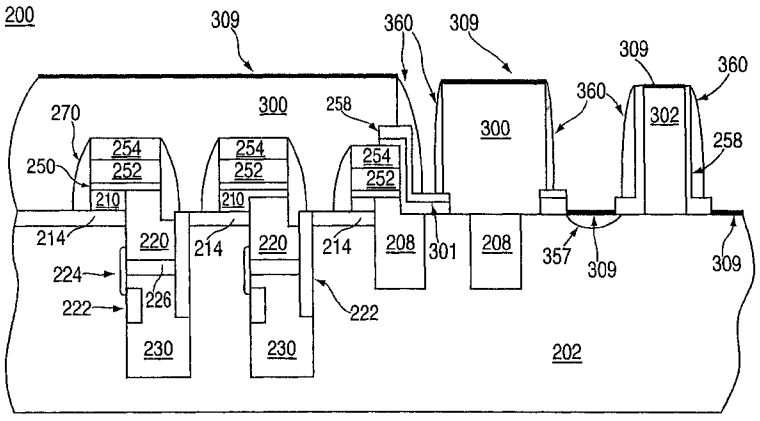
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(54) Title: STRUCTURE AND METHOD OF FABRICATING EMBEDDED VERTICAL DRAM ARRAYS WITH SILICIDED BITLINE AND POLYSILICON INTERCONNECT



(57) Abstract: A structure and process for fabricating embedded vertical DRAM cells includes fabricating vertical MOSFET DRAM cells with silicided polysilicon layers in the array regions, the landing pad and/or interconnect structures, the support source and drain regions and/or the gate stack. The process eliminates the need for a M0 metallization layer.

WO 03/005447 A3