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ABSTRACT

A METHOD TO FORM AND/OR ISOLATE VERTICAL TRANSISTORS

A method of fabricating an isolated vertical transistor comprising the following steps. A wafer having a first implanted region selected from the group comprising a source region and a drain region is provided. The wafer further includes STI areas on either side of a center transistor area. The wafer is patterned down to the first implanted region to form a vertical pillar within the center transistor area using a patterned hardmask. The vertical pillar having side walls. A pad dielectric layer is formed over the wafer, lining the vertical pillar. A nitride layer is formed over the pad dielectric layer. The structure is patterned and etched through the nitride layer and the pad dielectric layer; and into the wafer within the STI areas to form STI trenches within the wafer. The STI trenches are filled with insulative material to form STIs within STI trenches. The patterned nitride and pad dielectric layers are removed. The patterned hardmask is removed. Gate oxide is grown over the exposed portions of the wafer and the vertical pillar. Spacer gates are formed over the gate oxide lined side walls of the vertical pillar. Spacer gate implants are formed within the spacer gates, and a second implanted region is formed within the vertical pillar selected from the group consisting of a drain region and a source region that is not the same as the first implanted region to complete formation of the isolated vertical transistor.

FIGURE 2