We claim:

1. A semiconductor device comprising:

a package substrate including a lower surface and an upper surface, the lower surface including lower contacts for electrical connection to a circuit board;

an active structure formed on the upper surface of the package substrate, the active structure including thin-film transistors and upper contacts, the upper contacts being electrically connected with the thin-film transistors, the upper contacts being positioned on an upper surface of the active structure for electrical connection to a plurality of semiconductor dies; and

electrical interconnects connecting the lower contacts at the lower surface of the package substrate to the active structure at the upper surface of the package substrate;

wherein the thin-film transistors of the active structure form a circuit that is operable with another circuit provided by at least one of the plurality of semiconductor dies.

2. The semiconductor device of claim 1, wherein the thin-film transistors comprise non-silicon based thin-film transistors.

3. The semiconductor device of claim 1, wherein the active structure comprises multiple layers of interconnected thin-film transistors.

4. The semiconductor device of claim 1, wherein the thin-film transistors comprise lateral thin-film transistors.

5. The semiconductor device of claim 1, wherein the thin-film transistors comprise vertical thin-film transistors.

6. The semiconductor device of claim 1, wherein the electrical interconnects are formed in the package substrate.

7. The semiconductor device of claim 1, wherein the active structure further comprises a lower interconnect layer.

8. The semiconductor device of claim 7, wherein the electrical interconnects are formed in the lower interconnect layer.

9. The semiconductor device of claim 7, wherein the electrical interconnects are formed in both the package substrate and the lower interconnect layer of the active structure.

10. The semiconductor device of claim 7, wherein the lower interconnect layer includes conductive traces, vias, or both conductive traces and vias.

11. The semiconductor device of claim 1, wherein the active structure further comprises an upper interconnect layer to electrically connect the thin-film transistors to the upper contacts.

12. The semiconductor device of claim 11, wherein the upper interconnect layer includes conductive traces, vias, or both conductive traces and vias.

13. The semiconductor device of claim 1, wherein the upper contacts of the active structure comprise pads for solder balls to provide the electrical connection to the plurality of semiconductor dies.

14. The semiconductor device of claim 1, wherein the lower contacts of the package substrate comprise pads for solder balls to provide the electrical connection to the circuit board.

15. The semiconductor device of claim 1, wherein the lower contacts of the package substrate comprise pins to provide the electrical connection to the circuit board.

16. The semiconductor device of claim 1, wherein the active structure further comprises an adhesion layer to provide adhesion of the active structure to the package substrate.

17. The semiconductor device of claim 1, wherein the active structure further comprises

a combination of resistors, inductors, and/or capacitors that together with the thin-film transistors form the circuit of the active structure.

18. The semiconductor device of claim 1, wherein the circuit formed with the thin-film transistors further comprises one or more of:

an inverter;

a flip flop;

a register;

a power regulator;

a voltage converter;

a buck converter;

a buck-boost converter;

a voltage level shifter;

an amplifier;

a clock tree;

a clock tree fan out circuit; and

a port switching circuit.

19. The semiconductor device of claim 1, wherein the circuit formed with the thin-film transistors is configured to test operation of the circuit provided by the at least one of the plurality of semiconductor dies.

20. The semiconductor device of claim 1, wherein the circuit formed with the thin-film transistors is configured to verify operation of the circuit provided by the at least one of the plurality of semiconductor dies.

21. The semiconductor device of claim 1, wherein the package substrate comprises a phenolic or polymer.

22. A packaged semiconductor device comprising:

a package substrate;

an active structure formed on an upper surface of the package substrate, the active structure including non-silicon based active devices;

upper contacts at an upper surface of the active structure;

lower contacts at a lower surface of the package substrate for electrical connection to a circuit board;

electrical interconnects formed in the package substrate, the active structure, or both the package substrate and the active structure, the electrical interconnects interconnecting the lower contacts, the non-silicon based active devices of the active structure, and the upper contacts;

a plurality of semiconductor dies connected to the upper contacts; and

a package body encapsulating the package substrate, the active structure, and the plurality of semiconductor dies and exposing the lower contacts for electrical connection to the circuit board;

wherein the non-silicon based active devices of the active structure form a circuit that is operable with another circuit provided by at least one of the plurality of semiconductor dies.

23. The semiconductor device of claim 22, wherein the non-silicon based active devices comprise thin-film transistors.

24. The semiconductor device of claim 22, wherein the active structure comprises multiple layers of interconnected thin-film transistors.

25. The semiconductor device of claim 23, wherein the thin-film transistors comprise lateral thin-film transistors.

26. The semiconductor device of claim 23, wherein the thin-film transistors comprise vertical thin-film transistors.

27. The semiconductor device of claim 22, wherein the upper contacts comprise pads for solder balls to provide the electrical connection to the plurality of semiconductor dies.

28. The semiconductor device of claim 22, wherein the lower contacts comprise pads for solder balls to provide the electrical connection to the circuit board.

29. The semiconductor device of claim 22, wherein the lower contacts comprise pins to provide the electrical connection to the circuit board.

30. The semiconductor device of claim 22, wherein the active structure further comprises an adhesion layer to provide adhesion of the active structure to the package substrate.

31. The semiconductor device of claim 22, wherein the active structure further comprises a combination of resistors, inductors, and/or capacitors that together with the non-silicon based active devices form the circuit of the active structure.

32. The semiconductor device of claim 22, wherein the circuit formed with the non-silicon based active devices further comprises one or more of:

an inverter;

a flip flop;

a register;

a power regulator;

a voltage converter;

a buck converter;

a buck-boost converter;

a voltage level shifter;

an amplifier;

a clock tree;

a clock tree fan out circuit; and

a port switching circuit.

33. The semiconductor device of claim 22, wherein the circuit formed with the non-silicon based active devices is configured to test operation of the circuit provided by the at least one of the plurality of semiconductor dies.

34. The semiconductor device of claim 22, wherein the circuit formed with the non-silicon based active devices is configured to verify operation of the circuit provided by the at least one of the plurality of semiconductor dies.

35. The semiconductor device of claim 22, wherein the least one of the plurality of semiconductor dies comprises a processor or memory.

36. A packaged semiconductor device comprising:

a package substrate;

an active structure formed on an upper surface of the package substrate, the active structure including thin-film transistors;

upper contacts at an upper surface of the active structure;

lower contacts at a lower surface of the package substrate for electrical connection to a circuit board;

electrical interconnects formed in the package substrate, the active structure, or both the package substrate and the active structure, the electrical interconnects

interconnecting the lower contacts, the thin-film transistors of the active structure, and the upper contacts;

a plurality of semiconductor dies connected to the upper contacts; and

a package body encapsulating the package substrate, the active structure, and the plurality of semiconductor dies and exposing the lower contacts for electrical connection to the circuit board;

wherein the thin-film transistors of the active structure form a circuit that is operable with another circuit provided by at least one of the plurality of semiconductor dies.

37. A method of making a semiconductor device, the method comprising:

forming a package substrate, the package substrate including a lower surface and an upper surface, wherein the lower surface includes lower contacts for electrical connection to a circuit board;

forming a layer of thin-film transistors over the upper surface of the package substrate, including electrically connecting the thin-film transistors to the lower contacts, wherein the thin-film transistors are configured to form a circuit; and

forming upper contacts for electrically connecting at least one of a plurality of semiconductor dies to the circuit formed by the thin-film transistors, the upper contacts being formed over the layer of thin-film transistors or over an interconnect layer that is formed over the layer of thin-film transistors.

38. The method of claim 37, comprising forming multiple interconnected layers of thin-film transistors, including the layer of thin-film transistors, over the surface of the package substrate.

39. The method of claim 37, wherein the thin-film transistors comprise non-silicon based thin-film transistors.

40. The method of claim 37, further comprising electrically connecting the plurality of semiconductor dies to the upper contacts.

41. The method of claim 40, further comprising encapsulating the package substrate and the plurality of semiconductor dies in a package body.

42. The method of claim 37, wherein forming the layer of thin-film transistors over the surface of the package substrate comprises performing deposition.

43. The method of claim 42, wherein the deposition comprises atomic layer deposition, sputtering, chemical vapor deposition, or plasma enhanced chemical vapor deposition.

44. The method of claim 37, further comprising forming an adhesion layer on the surface of the package substrate to adhere the layer of thin-film transistors to the package substrate.

45. The method of claim 44, wherein forming the adhesion layer comprises performing atomic layer deposition, sputtering, or chemical vapor deposition.