What is claimed is:

1. A method of making a diode comprising:

forming a ~~first cladding layer~~ bottom diode region including one or more fins of polar crystalline material, wherein major faces of the one or more fins are non-polar;

forming an active diode region over one or more of said major faces; and

forming a ~~second cladding layer~~ top diode region adjacent to said active diode region.

~~2. A method of making a diode comprising:~~

~~providing a first cladding layer of a polar semiconductor crystalline material including a first surface with one or more holes formed therein, sidewalls of the one or more holes being non-polar faces of the polar semiconductor crystalline material;~~

~~providing a second cladding layer opposite the first surface; and~~

~~providing an active region interposed between the first and second cladding layers extending at least partially into the one or more holes.~~

~~3. A method of making a diode comprising:~~

~~forming a first diode region;~~

~~forming an active region adjacent the first diode region; and~~

~~forming a second diode region adjacent the active region, wherein an area of one or more surfaces of the first diode region adjacent the active region that are non-polar is greater than an area of one or more surfaces of the first diode region that are polar.~~

~~4. A method of making a light emitting diode comprising:~~

~~providing a first diode region;~~

~~forming an active diode region adjacent the first diode region; and~~

~~forming a second diode region adjacent the active diode region, wherein at least a portion of the active diode region and the second diode region correspond to a non-polar plane of the III-N semiconductor crystalline material.~~

~~5. A method of making a light emitting diode comprising:~~

~~providing a bottom diode region from a III-N semiconductor material;~~

~~forming an active diode region from a III-N semiconductor material adjacent the bottom diode region; and~~

forming a top diode region from a III-N semiconductor material adjacent the active diode region, wherein the active and top diode regions have fewer defects per unit area than the bottom diode region.

6. A method of making a light emitting diode comprising:

providing a bottom diode material;

forming a cavity in the bottom diode material;

forming an active diode region on a surface of the cavity; and

depositing a top diode material in the cavity.

7. A method of making a light emitting diode comprising:

providing bottom, active and top diode regions from III-N semiconductor material; and

providing non-polar III-N semiconductor material in the LED to increase an output efficiency to over a prescribed amount.

8. A method of making a light emitting diode comprising:

providing III-N semiconductor crystalline layer on a polar plane;

forming a bottom diode region having at least one first surface aligned in a non-polar plane and at least one second surface aligned in a polar plane of the III-N semiconductor material layer;

forming an active diode region adjacent the at least one first surface and the at least one second surface of the bottom diode region; and

forming a top diode region adjacent the active diode region.

9. A method of making a light emitting diode comprising:

providing a bottom diode region of III-N semiconductor material;

forming an active diode region adjacent the bottom diode region on a non-polar surface of III-N semiconductor material; and

forming a top diode region adjacent the active diode region.

10. A method of making a light emitting diode comprising:

providing a first diode region;

forming an active diode region adjacent the first diode region; and

forming a second diode region adjacent the active diode region, wherein a first portion of the active diode region has a first output light efficiency and a second portion of the active diode region has a second lower output

~~light efficiency.~~

~~11.~~2. The method of ~~one of~~ claims 1~~-10~~, wherein the active diode region is III-N semiconductor material corresponding to a non-polar surface.

~~12.~~3. The method of ~~one of~~ claims 1~~-10~~, wherein at least one of the active and top diode regions has more total line defects than the bottom diode region.

~~13. The method of one of claims 1-10, wherein a light output efficiency in a blue light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~14. The method of one of claims 1-10, wherein a light output efficiency in a green light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~15. The method of one of claims 1-10, wherein a light output efficiency in a white light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~16. The method of one of claims 1-10, wherein a light output efficiency in a ultraviolet light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~17. The method of one of claims 1-10, wherein a light output efficiency in an infrared light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~18.~~4. ~~-~~The method of ~~one of~~ claims 1~~-10~~, wherein a ratio of non-polar surface area in the bottom diode region facing the active diode region to polar-plane surface area is more than one.

~~19.~~5. The method of ~~one of~~ claims 1~~-10~~, wherein a ratio of non-polar surface area in the bottom diode region facing the active diode region to polar-plane surface area is more than 2, more than 4, more than 10 or more than 50.

~~20.~~6. The method of ~~one of~~ claims 1~~-10~~, wherein a portion of the active diode region oriented to a polar surface of III-N semiconductor material is less than 50%, less than 25%, less than 15%, less than 10% or less than 5%.

~~21.~~7. The method of ~~one of~~ claims 1~~-10~~, wherein a portion of the top diode region oriented to a polar surface of

III-N semiconductor material is less than 50%, less than 25%, less than 15%, less than 10% or less than 5%.

~~22.~~8. The method of ~~one of~~ claims ~~1-10~~, wherein a portion of the active diode region, the bottom diode region or the top diode region oriented to a polar surface of III-N semiconductor material is less than 50%, less than 25%, less than 15%, less than 10% or less than 5%.

~~23.~~9. The method of ~~one of~~ claims ~~1-10~~, wherein a portion of the active diode region, the bottom diode region or the top diode region oriented to a non-polar surface of III-N semiconductor material is greater than 50%, greater than 75%, greater than 85% or greater than 95%.

~~24.~~10. The method of ~~one of~~ claims ~~1-10~~, wherein the bottom and top diode regions include one or more of the following:

aluminum nitride (AlN), gallium nitride (GaN), indium nitride (InN), and their ternary and quaternary compounds.

~~25.~~11. The method of ~~one of~~ claims ~~1-10~~, wherein the bottom and top diode regions includes GaN.

~~26.~~12. The method of ~~one of~~ claims ~~1-10~~, wherein the bottom diode region is configured with an opening, wherein the opening is a trench, recess or hole.

~~27.~~13. The method of claim ~~26~~12, comprising a semiconductor device configured over at least a part of the opening.

~~28.~~14. The method of claims ~~26~~12, wherein the trench is at least 2 times deeper than its width, at least 5 times deeper than its width, at least 10 times deeper than its width or the trench is at least 100 times deeper than its width.

~~29.~~15. The method of claims ~~26~~12, wherein the trench is at least 10 times longer than its width or the trench is at least 100 times longer than its width.

~~30.~~16. The method of claim ~~26~~12, wherein the width of the openings is one of 450 nm or less, 400 nm or less, 350 nm or less, 200 nm or less, 100 nm or less and 50 nm or less.

~~31.~~17. The method of claim ~~26~~12, wherein the width of the openings is one of 5 um or less, 2 um or less and 1 um

or less.

~~32.~~18. The method of ~~one of~~ claims 1-~~10~~, wherein the bottom and top diode regions are epitaxially grown.

~~33.~~19. The method of ~~one of~~ claims 1-~~10~~, further comprising a CMOS device integrated with a substrate.

~~34.~~20. The method of ~~one of~~ claims 1-~~10~~, wherein a substrate comprises silicon, germanium or sapphire.

~~35.~~21. The method of claim ~~34~~20, wherein a surface of the substrate exposed in the insulator pattern opening is a (100) surface of the silicon substrate, and wherein the substrate is a single crystal substrate ~~or a polycrystalline substrate~~.

~~36.~~22. The method of ~~one of~~ claims 1-~~10~~, wherein the bottom, active and top diode regions are the same semiconductor crystalline material.

~~37.~~23. The method of ~~one of~~ claims 1-~~10~~, wherein the bottom region is a different semiconductor crystalline material than at least the active diode region or the top diode region.

~~38.~~24. The method of ~~one of~~ claims 1-~~10~~, wherein the bottom and top diode regions are doped with different doping concentrations.

~~39.~~25. The method of ~~one of~~ claims 1-~~10~~, wherein the top and active diode regions are doped with different doping concentrations.

~~40.~~26. The method of ~~one of~~ claims 1-~~10~~, wherein the bottom and top diode regions are doped with dopants of different types.

~~41.~~27. The method of ~~one of~~ claims 1-~~10~~, wherein the bottom and top diode regions are in situ doped or ion implanted.

~~42.~~28. The method of ~~one of~~ claims 1-~~10~~, wherein at least one of the active and top diode regions are formed by selective epitaxial growth including metal-organic chemical vapor deposition (MOCVD), atmospheric-pressure CVD (APCVD), low- (or reduced-) pressure CVD (LPCVD), ultra-high-vacuum CVD (UHVCVD), molecular beam

epitaxy (MBE), or atomic layer deposition (ALD).

~~43.~~29. The method of ~~one of~~ claims 1~~-10~~, wherein the bottom, active and top diode regions are repeated.

~~44.~~30. The method of ~~one of~~ claims 1~~-10~~, wherein at least a portion of the active diode region corresponding to a polar face is removed.

~~45.~~31. The method of ~~one of~~ claims 1~~-10~~, wherein at least a portion of the bottom diode region or the top diode region corresponding to a polar face is removed.

~~46.~~32. The method of ~~one of~~ claims 1~~-10~~, comprising an intrinsic active region.

~~47.~~33. The method of ~~one of~~ claims 1~~-10~~, wherein the active diode region comprises a depletion region.

~~48.~~34. A method of manufacturing an LED comprising the method of ~~one of~~ claims 1~~-10~~.

~~49.~~35. A method of manufacturing a laser diode comprising the method of ~~one of~~ claims 1~~-10~~.

~~50.~~36. A method of manufacturing a photovoltaic device comprising the method of ~~one of~~ claims 1~~-10~~.

~~51.~~37. A diode comprising:

one or more fins of polar crystalline material, wherein major faces of the one or more fins are non-polar, said one or more fins constituting a ~~first cladding layer~~ bottom diode region;

an active diode region formed around said one or more fins; and

a ~~second cladding layer~~ top diode region formed adjacent to said active diode region.

~~52. A diode comprising:~~

~~a first cladding layer of a polar crystalline material including a first surface with one or more holes therein, sidewalls of the one or more holes being non-polar faces of the polar crystalline material;~~

~~a second cladding layer opposite the first surface and extending at least partially into the one or more holes; and~~

~~an active region interposed between the first and second cladding layers.~~

~~53. A diode comprising:~~

~~a first diode region;~~

~~an active region adjacent the first diode region; and~~

~~a second diode region adjacent the active region, wherein an area of one or more surfaces of the first diode region adjacent the active region that are non-polar is greater than an area of one or more surfaces of the first diode region that are polar.~~

~~54. A light emitting diode comprising:~~

~~a first diode region;~~

~~an active diode region of a III-N semiconductor crystalline material adjacent the first diode region; and~~

~~a second diode region adjacent the active diode region, wherein at least a portion of the active diode region corresponds to a non-polar plane of the first diode region.~~

~~55. A light emitting diode comprising:~~

~~a bottom diode region from a III-N semiconductor material;~~

~~an active diode region from a III-N semiconductor material adjacent the bottom diode region; and~~

~~a top diode region from a III-N semiconductor material adjacent the active diode region, wherein the active and top diode regions have fewer defects per unit area than the bottom diode region.~~

~~56. A light emitting diode comprising:~~

~~a bottom diode material having a cavity therein;~~

~~an active diode region on a surface of the cavity; and~~

~~depositing a top diode material in the cavity.~~

~~57. A light emitting diode comprising:~~

~~bottom, active and top diode regions from III-N semiconductor material, wherein non-polar III-N semiconductor material in the LED is configured to increase an output efficiency.~~

~~58. A light emitting diode comprising:~~

~~a bottom diode region of III-N semiconductor crystalline layer on a polar plane having at least one first surface aligned in a non-polar plane and at least one second surface aligned in a polar plane of the III-N semiconductor material layer;~~

~~an active diode region adjacent the at least one first surface and the at least one second surface of the bottom diode region; and~~

~~a top diode region adjacent the active diode region.~~

~~59. A light emitting diode comprising:~~

~~a bottom diode region of III-N semiconductor material;~~

~~an active diode region adjacent the bottom diode region on a non-polar surface of III-N semiconductor material; and~~

~~a top diode region adjacent the active diode region.~~

~~60. A light emitting diode comprising:~~

~~a first diode region;~~

~~an active diode region adjacent the first diode region; and~~

~~a second diode region adjacent the active diode region, wherein a first portion of the active diode region has a first output light efficiency and a second portion of the active diode region has a second lower output light efficiency.~~

~~61.~~38. The diode of ~~one of~~ claims ~~51-~~37~~60~~, wherein the active diode region is III-N semiconductor material corresponding to a non-polar surface.

~~62.~~39. The diode of ~~one of~~ claims ~~51~~37~~-60~~, wherein at least one of the active and top diode regions has more total line defects than the bottom diode region.

~~63. The diode of one of claims 51-60, wherein a light output efficiency in a blue light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~64. The diode of one of claims 51-60, wherein a light output efficiency in a green light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~65. The diode of one of claims 51-60, wherein a light output efficiency in a white light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~66. The diode of one of claims 51-60, wherein a light output efficiency in a ultraviolet light LED is more than 2~~

~~times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~67. The diode of one of claims 51-60, wherein a light output efficiency in an infrared light LED is more than 2 times greater, more than 5 times greater, more than 10 times greater or more than 25 times greater.~~

~~68.~~40. ~~The~~ The diode of ~~one of~~ claims ~~51~~ 37-~~60~~, wherein a ratio of non-polar surface area in the bottom diode region facing the active diode region to polar-plane surface area is more than one.

~~69.~~41. The diode of ~~one of~~ claims ~~51~~ 37-~~60~~, wherein a ratio of non-polar surface area in the bottom diode region facing the active diode region to polar-plane surface area is more than 2, more than 4, more than 10 or more than 50.

~~70.~~42. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein a portion of the active diode region oriented to a polar surface of III-N semiconductor material is less than 50%, less than 25%, less than 15%, less than 10% or less than 5%.

~~71.~~43. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein a portion of the top diode region oriented to a polar surface of III-N semiconductor material is less than 50%, less than 25%, less than 15%, less than 10% or less than 5%.

~~72.~~44. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein a portion of the active diode region, the bottom diode region or the top diode region oriented to a polar surface of III-N semiconductor material is less than 50%, less than 25%, less than 15%, less than 10% or less than 5%.

~~73.~~45. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein a portion of the active diode region, the bottom diode region or the top diode region oriented to a non-polar surface of III-N semiconductor material is greater than 50%, greater than 75%, greater than 85% or greater than 95%.

~~74.~~46. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom and top diode regions include one or more of the following:

aluminum nitride (AlN), gallium nitride (GaN), indium nitride (InN), and their ternary and quaternary compounds.

~~75.~~47. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom and top diode regions includes GaN.

~~76.~~48. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom diode region is configured with an opening,

wherein the opening is a trench, recess or hole.

~~77.~~49. The diode of claim ~~76~~48, comprising a semiconductor device configured over at least a part of the opening.

~~78.~~50. The diode of claim ~~76~~48, wherein the trench is at least 2 times deeper than its width, at least 5 times deeper than its width, at least 10 times deeper than its width or the trench is at least 100 times deeper than its width.

~~79.~~51. The diode of claim ~~76~~48, wherein the trench is at least 10 times longer than its width or the trench is at least 100 times longer than its width.

~~80.~~52. The diode of claim ~~76~~48, wherein the width of the openings is one of 450 nm or less, 400 nm or less, 350 nm or less, 200 nm or less, 100 nm or less and 50 nm or less.

~~81.~~53. The diode of claim ~~76~~48, wherein the width of the openings is one of 5 um or less, 2 um or less and 1 um or less.

~~82.~~54. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom and top diode regions are epitaxially grown.

~~83.~~55. The diode of ~~one of~~ claims ~~51~~37-~~60~~, further comprising a CMOS device integrated with a substrate.

~~84.~~56. The diode of ~~one of~~ claim ~~51~~37-~~60~~, wherein a substrate comprises silicon, germanium or sapphire.

~~85.~~57. The diode of claim ~~84~~56, wherein a surface of the substrate exposed in the insulator pattern opening is a (100) surface of the silicon substrate, and wherein the substrate is a single crystal substrate ~~or a polycrystalline substrate~~.

~~86.~~58. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom, active and top diode regions are the same semiconductor crystalline material.

~~87.~~59. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom diode region is a different semiconductor crystalline material than at least the active diode region or the top diode region.

~~88.~~60. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom and top diode regions are doped with different doping concentrations.

~~89.~~61. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the top and active diode regions are doped with different doping concentrations.

~~90.~~62. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom and top diode regions are doped with dopants of different types.

~~91.~~63. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom and top diode regions are in situ doped or ion implanted.

~~92.~~64. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein at least one of the active diode region and top diode region are formed by selective epitaxial growth including metal-organic chemical vapor deposition (MOCVD), atmospheric-pressure CVD (APCVD), low- (or reduced-) pressure CVD (LPCVD), ultra-high-vacuum CVD (UHVCVD), molecular beam epitaxy (MBE), or atomic layer deposition (ALD).

~~93.~~65. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the bottom, active and top diode regions are repeated.

~~94.~~66. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein at least a portion of the active diode region corresponding to a polar face is removed.

~~95.~~67. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein at least a portion of the bottom diode region or the top diode region corresponding to a polar face is removed.

~~96.~~68. The diode of ~~one of~~ claims ~~51~~37-~~60~~, comprising an intrinsic active region.

~~97.~~69. The diode of ~~one of~~ claims ~~51~~37-~~60~~, wherein the active diode region comprises a depletion region.

~~98.~~70. An LED comprising the diode of ~~one of~~ claims ~~51~~37-~~60~~.

~~99.~~71. A laser diode comprising the diode of ~~one of~~ claims ~~51~~37-~~60~~.

~~100.~~72. A photovoltaic device comprising the diode of ~~one of~~ claims ~~51~~37-~~60~~.