

DESCRIPTION

TITLE:

TILED DISPLAY PANEL

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BACKGROUND

Technical Field

[0001] The disclosure relates to a display panel, and in particular to a tiled display panel.

10 Description of Related Art

[0002] Limited by the physical limitations of semiconductor technology, the panel sizes that can be quantified by LCD panel factories today are still limited. The main reason is that the higher the size of the panel, the higher the cost and the lower the yield. As a result, the higher the size of the panel, the lower the supply. However, given the significant
15 benefits of LCD panels in advertising and marketing, the demand of the market for large panels is becoming increasingly intense. Therefore, using panels of existing sizes for further assembling into large panels is now a feasible way to achieve large panels.

[0003] With the advancement of packaging technology, the borders of LCD panels have become very narrow. However, when the panels are tiled together, the tiled lines between
20 the panels make the frame discontinuous, which affects the viewing experience. Therefore, how to achieve seamless tiling of tiled display panels is an important issue to improve the viewing experience.

SUMMARY

[0004] The disclosure provides a tiled display panel which can shorten the undisplayable frame of a liquid crystal panel to achieve a purpose of seamless tiling of the tiled display panel.

5 **[0005]** A tiled display panel of the disclosure includes multiple substrates, multiple liquid crystal pixels, multiple light-emitting diode (LED) pixels, and multiple light-emitting circuits. Each of the substrates has a display region and a boundary region. The boundary region is respectively located between the display region and a tiled boundary tiled by the substrates. The liquid crystal pixels are arranged in an array in the display
10 region. The LED pixels are arranged in an array in the boundary region. The light-emitting circuits are arranged in series in the boundary region along a first direction and are electrically connected to the LED pixels to provide multiple light-emitting signals for the LED pixels.

[0006] A tiled display panel of the disclosure includes multiple substrates, multiple liquid
15 crystal pixels, and multiple light-emitting driving line. Each of the substrates has a display region and a boundary region. The boundary region is respectively located between the display region and a tiled boundary tiled by the substrate. The liquid crystal pixels are arranged in an array in the display region. The LED pixels are arranged in an array in the boundary region. The light-emitting driving lines receive multiple light-emitting signals,
20 span the boundary region along a first direction, and are electrically connected to the LED pixels to provide the light-emitting signals for the LED pixels.

[0007] Based on the above, in the tiled display panel according to the embodiment of the disclosure, the LED pixels may be lit up based on the light-emitting signal of the light-emitting circuit. In this way, the LED pixels may be driven normally, and the seamless

tilled effect can be achieved by taking the advantage of the borderless LED pixel.

[0008] In order to make the above-mentioned features and advantages of the disclosure comprehensible, embodiments are given below and described in detail with reference to the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a schematic system diagram of a display device according to an embodiment of the disclosure.

[0010] FIG. 2A to FIG. 2D are schematic wiring diagrams of a tiled display panel
10 according to an embodiment of the disclosure.

[0011] FIG. 3 is a schematic circuit diagram of a liquid crystal pixel according to an embodiment of the disclosure.

[0012] FIG. 4 is a schematic circuit diagram of an LED pixel according to an embodiment of the disclosure.

15 **[0013]** FIG. 5 is a schematic circuit diagram of an LED pixel according to an embodiment of the disclosure.

[0014] FIG. 6 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure.

[0015] FIG. 7 is a schematic circuit diagram of a light-emitting circuit according to an
20 embodiment of the disclosure.

[0016] FIG. 8 is a schematic wiring diagram of a tiled display panel according to an embodiment of the disclosure.

[0017] FIG. 9 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure.

[0018] FIG. 10 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure.

[0019] FIG. 11 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure.

5 **[0020]** FIG. 12 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure.

[0021] FIG. 13A is a schematic wiring diagram of a tiled display panel according to an embodiment of the disclosure.

[0022] FIG. 13B is a schematic diagram of driving waveforms of a tiled display panel
10 according to an embodiment of the disclosure.

[0023] FIG. 13C is a schematic diagram of driving waveforms of a tiled display panel according to an embodiment of the disclosure.

[0024] FIG. 14 is a schematic wiring diagram of a tiled display panel according to an embodiment of the disclosure.

15 **[0025]** FIG. 15 is a schematic wiring diagram of a tiled display panel according to an embodiment of the disclosure.

DESCRIPTION OF THE EMBODIMENTS

[0026] Unless otherwise defined, all terms (including technical and scientific terms) used
20 herein have the same meaning as commonly understood by one of ordinary skill in the art to which the disclosure belongs. It is further understood that terms such as those defined in commonly used dictionaries should be interpreted as having meanings consistent with the relevant art and the background or context of the disclosure, and should not to be interpreted in an idealized or overly formal manner, unless otherwise defined in the embodiments of

the disclosure.

[0027] It should be understood that, although the terms “first”, “second”, “third”, etc. may be used herein to describe various elements, components, regions, layers, and/or portions, these elements, components, regions, layers, and/or portions should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer, or portion from another element, component, region, layer, or portion. Thus, a “first element”, “component”, “region”, “layer”, or “portion” discussed below could be termed a second element, component, region, layer, or portion without departing from the teachings herein.

[0028] The terminologies used herein are only for the purpose of describing particular embodiments and are not restrictive. As used herein, the singular forms “a,” “an,” and “the” are intended to include the plural forms including “at least one” or represent “and/or” unless the content clearly indicates otherwise. As used herein, the terminology “and/or” includes any and all combinations of one or more of the associated listed items. It should also be understood that when used in this disclosure, the terminologies “include” and/or “comprise” indicate the presence of the described features, regions, overall scenarios, steps, operations, elements, and/or components but do not exclude the presence or addition of one or more other features, regions, overall scenarios, steps, operations, elements, components, and/or combinations thereof.

[0029] FIG. 1 is a schematic system diagram of a display device according to an embodiment of the disclosure. Please refer to FIG. 1. In this embodiment, a display device 10 includes multiple tiled display panels 100, multiple control substrates (such as 11 and 11’), and multiple thin-film substrates (such as 12 and 12’). The tiled display panel 100 includes multiple substrates (here, two substrates 101 and 102 are taken as an example),

multiple liquid crystal pixels PXCX, a multiple LED pixels (multiple red LED pixels PDR, multiple green LED pixels PDG, and multiple blue LED pixels PDB are taken as an example), multiple light-emitting circuits CTem, multiple first gate lines LX1, and multiple second gate lines LX2. The liquid crystal pixel PXCX is driven by voltage, and the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB are driven by a current. Moreover, the thin-film substrate (such as 12 and 12') is configured to be electrically connected to the tiled display panel 100 and the control substrate (such as 11 and 11').

[0030] In this embodiment, each substrate (such as 101 and 102) has a display region (such as 110 and 110'), at least one boundary region (such as 120 and 120'), and a fan-in region (such as 130 and 130'). The number of boundary regions (such as 120 and 120') depends on the tiled requirements of the substrate (101 and 102), and the boundary region (such as 120 and 120') are respectively located between the display region (such as 110 and 110') and the tiled boundary Etile tiled by the substrates 101 and 102. The liquid crystal pixels PXCX are arranged in an array in the display region (such as 110 and 110'), and the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB are arranged in an array in the boundary region (such as 120 and 120'). The light-emitting circuits CTem are arranged in series in the boundary region (such as 120 and 120') along a first direction D1, and are electrically connected to the red LED pixels PDR, the green LED pixels PDG, and the blue LED pixels PDB to provide multiple light-emitting signals em for the red LED pixels PDR, the green LED pixels PDG, and the blue LED pixels PDB.

[0031] Taking the substrate 101 as an example, the first gate line LX1 spans the display region 110 along the first direction D1 and receives multiple gate signals GX enabled in sequence. The second gate line LX2 spans the display region 110 and the boundary region

120 along the second direction D2 perpendicular to the first direction D1. Each second gate line LX2 is electrically connected to one of the first gate lines LX1 (for example, through a hole), a row (or part) of liquid crystal pixels PXCX, a row (or part) of red LED pixels PDR, green LED pixels PDG, and blue LED pixels PDB to transmit the gate signal
5 GX to the liquid crystal pixel PXCX, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB.

[0032] Based on the above, the liquid crystal pixel PXCX, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB may write data voltage based on the gate signal (such as GX) transmitted by the second gate line (such as LX2). Moreover, the
10 red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB may be lit up based on the light-emitting signal em of the light-emitting circuit CTem. In this way, the liquid crystal pixel PXCX, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB may be driven normally, and the seamless tiled effect may be achieved by taking the advantage of no boundaries of the red LED pixel PDR, the green LED pixel PDG,
15 and the blue LED pixel PDB.

[0033] In this embodiment, the light-emitting circuits CTem are arranged in series between the red LED pixels PDR, the green LED pixels PDG, the blue LED pixels PDB, and the tiled boundary Etile.

[0034] In this embodiment, a control circuit (such as a timing controller) may be disposed
20 on the control substrate (such as 11 and 11'), and a driving circuit (such as a gate driver and source driver) may be disposed on the thin-film substrate (such as 12 and 12'). Further, the circuits on the control substrate 11 and the thin-film substrate 12 are configured to drive the liquid crystal pixel PXCX, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB on the substrate 101. Moreover, the circuits on the control substrate

11' and the thin-film substrate 12' are configured to drive the liquid crystal pixel PXCX, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB on the substrate 102.

[0035] In this embodiment, the material of the substrates 101 and 102 includes one of a
5 P-type amorphous silicon (a-Si) substrate, an N-type a-Si substrate, an indium gallium zinc oxide (IGZO) substrate, and a low-temperature polycrystalline silicon (LTPS) substrate.

[0036] In the embodiment of the disclosure, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB may be arranged in sequence. For example, starting from the tiled boundary Etile, the first column may be the red LED pixel PDR, and the
10 second column may be the green LED pixel PDG, and the third column may be the blue LED pixel PDB. Alternatively, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB may be arranged obliquely. For example, the first row is the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB arranged in sequence, the second row is the green LED pixel PDG, the blue LED pixel PDB, and the
15 red LED pixel PDR arranged in sequence, the third row is the blue LED pixel PDB, the red LED pixel PDR, and the green LED pixel PDG arranged in sequence, and so on. Moreover, the arrangement of the colors of the liquid crystal pixels PXCX (that is, the color filters) is essentially aligned with the arrangement of the red LED pixels PDR, the green LED pixels PDG, and the blue LED pixels PDB, but the embodiment of the disclosure is
20 not limited thereto.

[0037] In the embodiment of the disclosure, three adjacent red LED pixel PDR, green LED pixel PDG, and blue LED pixel PDB may be integrated into one LED die Dled to facilitate transfer to the substrate (such as 101 and 102).

[0038] In this embodiment, in order to match the number of first gate lines LX1 and the

number of second gate lines LX2, part of the first gate line LX1 is not electrically connected to the second gate line LX2, or part of the first gate line LX1 may be omitted, but the embodiment of the disclosure is not limited thereto.

[0039] FIG. 2A to FIG. 2D are schematic wiring diagrams of a tiled display panel according to an embodiment of the disclosure. Please refer to FIG. 1 and FIG. 2A. In this embodiment, taking the substrate 101 as an example, the first gate line (such as LX1(n-2)~LX1(n+3)) of the display region 110 receives the gate signal (such as GX(n-2)~GX(n+3)), and the second gate line (such as LX2(n-2)~LX2(n+3)) is electrically connected to the first gate line (such as LX1(n-2)~LX1(n+3)).

[0040] In addition to the light-emitting circuit (such as CTem(n-2)~CTem(n+3)), the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB, multiple first break over line Ltu1 may be disposed in the boundary region 120, be electrically connected to one of the second gate lines (such as LX2(n-2)~LX2(n+3)) respectively, and extend along the first direction D1 respectively to be electrically connected to a first-level light-emitting circuit and a next-level light-emitting circuit of the light-emitting circuit (such as CTem(n-2)~CTem(n+3)), where n is a directive number.

[0041] For example, the first break over line Ltu1 electrically connected to the second gate line LX2(n) extends bidirectionally along the first direction D1 (that is, extending up and down simultaneously) to be electrically connected to the light-emitting circuit CTem(n-2) (that is, the first two levels of the light-emitting circuit CTem) and the light-emitting circuit CTem(n+2) (that is, the next two levels of the light-emitting circuit CTem), but the embodiment of the disclosure is not limited thereto. In other words, the first break over line Ltu1 may be electrically connected to the first three levels of the light-emitting circuit CTem and the next one level of the light-emitting circuit CTem, or the first break over line

Ltu1 may be electrically connected to the first one level of the light-emitting circuit C_{Tem} and the next three levels of the light-emitting circuit C_{Tem}, which depends on the circuit design. Based on the above, the configuration direction of the first-level light-emitting circuit C_{Tem} relative to the second gate line (such as LX2(n-2)~LX2(n+3)) electrically connected to each first break over line Ltu1 is opposite to the configuration direction of the next-level light-emitting circuit C_{Tem} relative to the second gate line (such as LX2(n-2)~LX2(n+3)) electrically connected to each first break over line Ltu1.

[0042] In this embodiment, the first break over line Ltu1 is elbow-shaped, and the first break over line Ltu1 is disposed between the light-emitting circuit (such as C_{Tem}(n-2)~C_{Tem}(n+3)) and the tiled boundary E_{tile}.

[0043] Please refer to FIG. 1, FIG. 2A, and FIG. 2B, where the same or similar elements use the same or similar reference numerals. In this embodiment, taking the substrate 101 as an example, a third gate line (such as LX3(n-2)~LX3(n+3)) may be disposed in the display region 110, and multiple second break over line lines Ltu2 may be disposed in the boundary region 120.

[0044] The third gate line (such as LX3(n-2)~LX3(n+3)) spans the display region 110 and the boundary region 120 along a second direction D2. Each third gate line (such as LX3(n-2)~LX3(n+3)) is located between two adjacent second gate lines (such as LX2(n-2)~LX2(n+3)), and is electrically connected to one (such as through a hole) of the first gate lines (such as LX1(n-2)~LX1(n+3)) and one of the light-emitting circuits (such as C_{Tem}(n-2)~C_{Tem}(n+3)). The second break over line Ltu2 is electrically connected to one of the second gate lines (such as LX2(n-2)~LX2(n+3)) respectively, and extends along the first direction D1 to be electrically connected to the first-level light-emitting circuit of the light-emitting circuit (such as C_{Tem}(n-2)~C_{Tem}(n+3)) respectively.

[0045] For example, the second break over line Ltu2 electrically connected to the second gate line LX2(n) extends up along the first direction D1 to be electrically connected to the light-emitting circuit CTem(n-2) (that is, the first two levels of the light-emitting circuit CTem), but the embodiment of the disclosure is not limited thereto. In other words, the second break over line Ltu2 may be electrically connected to the first three levels of the light-emitting circuit CTem, or the second break over line Ltu2 may be electrically connected to the first one level of the light-emitting circuit CTem, which depends on the circuit design.

[0046] In this embodiment, the first gate line (such as LX1(n-2)~LX1(n+3)) electrically connected to each third gate line (such as LX3(n-2)~LX3(n+3)) is closer to the boundary region 120 than the first gate line (such as LX1(n-2)~LX1(n+3)) electrically connected to the adjacent second gate line (such as LX2(n-2)~LX2(n+3)).

[0047] For example, the first gate line LX1(n-2) electrically connected to the third gate line LX3(n) is closer to the boundary region 120 than the first gate line LX1(n) electrically connected to the second gate line LX2(n) and the first gate line LX1(n-1) electrically connected to the second gate line LX2(n-1).

[0048] In this embodiment, the second break over line Ltu2 is elbow-shaped, and the second break over line Ltu2 is disposed between the light-emitting circuit (such as CTem(n-2)~CTem(n+3)) and the tiled boundary Etile.

[0049] Please refer to FIG. 1, FIG. 2A, and FIG. 2C, where the same or similar elements use the same or similar reference numerals. In this embodiment, taking the substrate 101 as an example, a fourth gate line (such as LX4(n-2)~LX4(n+3)) may be disposed in the display region 110, and multiple third break over lines Ltu3 may be disposed in the boundary region 120.

[0050] The fourth gate line (such as $LX4(n-2) \sim LX4(n+3)$) spans the display region 110 and the boundary region 120 along the second direction D2. Each fourth gate line (such as $LX4(n-2) \sim LX4(n+3)$) is located between two adjacent second gate lines (such as $LX2(n-2) \sim LX2(n+3)$), and is electrically connected to one (such as through a hole) of the first gate lines (such as $LX1(n-2) \sim LX1(n+3)$) and one of the light-emitting circuits (such as $CTem(n-2) \sim CTem(n+3)$). The third break over line Ltu3 is electrically connected to one of the second gate lines (such as $LX2(n-2) \sim LX2(n+3)$) respectively, and extends along the first direction D1 to be electrically connected to the next-level light-emitting circuit of the light-emitting circuit (such as $CTem(n-2) \sim CTem(n+3)$) respectively.

[0051] For example, the third break over line Ltu3 electrically connected to the second gate line $LX2(n)$ extends down along the first direction D1 to be electrically connected to the light-emitting circuit $CTem(n+2)$ (that is, the next two levels of the light-emitting circuit CTem), but the embodiment of the disclosure is not limited thereto. In other words, the third break over line Ltu3 may be electrically connected to the next three levels of the light-emitting circuit CTem, or the third break over line Ltu3 may be electrically connected to the next one level of the light-emitting circuit CTem, which depends on the circuit design.

[0052] In this embodiment, the first gate line (such as $LX1(n-2) \sim LX1(n+3)$) electrically connected to each fourth gate line (such as $LX4(n-2) \sim LX4(n+3)$) is further away from the boundary region 120 than the first gate line (such as $LX1(n-2) \sim LX1(n+3)$) electrically connected to the adjacent second gate line (such as $LX2(n-2) \sim LX2(n+3)$).

[0053] For example, the first gate line $LX1(n+2)$ electrically connected to the fourth gate line $LX4(n)$ is further away from the boundary region 120 than the first gate line $LX1(n)$ electrically connected to the second gate line $LX2(n)$ and the first gate line $LX1(n+1)$ electrically connected to the second gate line $LX2(n+1)$.

[0054] In this embodiment, the third break over line Ltu3 is elbow-shaped, and the third break over line Ltu3 is disposed between the light-emitting circuit (such as C_{Tem}(n-2)~C_{Tem}(n+3)) and the tiled boundary E_{tile}.

[0055] Please refer to FIG. 1 and FIG. 2A to FIG. 2D, where the same or similar elements use the same or similar reference numerals. In this embodiment, taking the substrate 101 as an example, the third gate line (such as LX3(n-2)~LX3(n+3)) and the fourth gate line (such as LX4(n-2)~LX4(n+3)) (corresponding to a fifth gate line and a sixth gate line) may be disposed in the display region 110, but no break over line is disposed in the boundary region 120. The configuration of the third gate line (such as LX3(n-2)~LX3(n+3)) and the fourth gate line (such as LX4(n-2)~LX4(n+3)) may be referred to FIG. 2B and FIG. 2C, which is not described again here.

[0056] FIG. 3 is a schematic circuit diagram of a liquid crystal pixel according to an embodiment of the disclosure. Please refer to FIG. 1 and FIG. 3. In this embodiment, the liquid crystal pixel PXCX takes a liquid crystal pixel PXCXa as an example, and the liquid crystal pixel PXCXa includes a switch transistor T_{cx}, a first pixel capacitance C_{x1}, and a second pixel capacitance C_{x2}. The switch transistor T_{cx} has a first terminal receiving a pixel data voltage Data, a control terminal receiving a gate signal GX(n) (corresponding to a first gate signal), and a second terminal. The first pixel capacitance C_{x1} is coupled between the second terminal of the switch transistor T_{cx} and a first common terminal CF-COM. The second pixel capacitance C_{x2} is coupled between the second terminal of the switch transistor T_{cx} and a second common terminal Array-COM.

[0057] FIG. 4 is a schematic circuit diagram of an LED pixel according to an embodiment of the disclosure. Please refer to FIG. 1 and FIG. 4. In this embodiment, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB take a LED pixel PDXa

as an example, and the LED pixel PDXa includes a LED XLED, transistors T11~T13 (corresponding to a first transistor to a third transistor), and a capacitance C11 (corresponding to a first capacitance). The transistors T11~T13 take an N-type transistor as an example, and the LED XLED may be the red LED, the green LED, or the blue LED.

5 **[0058]** The LED XLED has an anode and a cathode receiving a system low voltage VSS. The transistor T11 has a first terminal receiving the pixel data voltage Data, a control terminal receiving the gate signal GX(n), and a second terminal. The transistor T12 has a first terminal receiving the system high voltage VDD, a control terminal coupled to the second terminal of the transistor T11, and a second terminal. The transistor T13 has a first
10 terminal coupled to the second terminal of the transistor T12, a control terminal receiving the light-emitting signal EM(n) (that is, a corresponding one of the light-emitting signals em), and a second terminal coupled to the anode of the LED. The capacitance C11 is coupled between the control terminal of the transistor T12 and the second terminal of the transistor T12.

15 **[0059]** FIG. 5 is a schematic circuit diagram of an LED pixel according to an embodiment of the disclosure. Please refer to FIG. 1 and FIG. 5. In this embodiment, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB take a LED pixel PDXb as an example, and the LED pixel PDXb includes a LED XLED, transistors T21~T25 (corresponding to a fourth transistor to an eighth transistor), and a capacitance C21
20 (corresponding to a second capacitance). The transistors T21~T25 take a P-type transistor as an example, and the LED XLED may be the red LED, the green LED, or the blue LED.

[0060] The LED XLED has an anode and a cathode receiving the system low voltage VSS. The transistor T21 has a first terminal receiving the pixel data voltage Data, a control terminal receiving the gate signal GX(n), and a second terminal. The transistor T22 has a

first terminal, a control terminal coupled to the second terminal of the transistor T21, and a second terminal. The capacitance C21 is coupled between the first terminal of transistor T21 and the control terminal of the transistor T22. The transistor T23 has a first terminal receiving a reference voltage Vref, a control terminal receiving the gate signal GX(n), and
5 a second terminal coupled to the first terminal of the transistor T22.

[0061] The transistor T24 has a first terminal receiving the system high voltage VDD, a control terminal receiving the light-emitting signal EM(n), and a second terminal coupled to the first terminal of the transistor T22. The transistor T25 has a first terminal coupled to the second terminal of the transistor T22, a control terminal receiving the light-emitting
10 signal EM(n), and a second terminal coupled to the anode of the LED XLED.

[0062] FIG. 6 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure. Please refer to FIG. 1 and FIG. 6. In this embodiment, the light-emitting circuit CTem takes a light-emitting circuit CTema as an example, and the light-emitting circuit CTema includes transistors T31 and T32 (corresponding to a ninth
15 transistor and a tenth transistor). The transistors T31~T32 take the N-type transistor as an example.

[0063] The transistor T31 has a first terminal receiving a gate high voltage VGH, a control terminal receiving the gate signal GX(ny) (corresponding to a second gate signal), and a second terminal providing (or coupled to) the light-emitting signal EM(n). The transistor
20 T32 has a first terminal coupled to the second terminal of the transistor T31, a control terminal receiving the gate signal GX(nx) (corresponding to a third gate signal), and a second terminal that receiving a gate low level VGL. In this embodiment, x and y may be a positive integer, and x may be different from y.

[0064] FIG. 7 is a schematic circuit diagram of a light-emitting circuit according to an

embodiment of the disclosure. Please refer to FIG. 1 and FIG. 7. In this embodiment, the light-emitting circuit C_{Tem} takes a light-emitting circuit C_{Temb} as an example, and the light-emitting circuit C_{Temb} includes transistors T41~T43 and a capacitance C41. The transistors T41~T43 take the P-type transistor as an example.

5 **[0065]** The transistor T41 has a first terminal coupled to the light-emitting signal EM(n), a control terminal receiving the gate signal GX(n), and a second terminal receiving the gate high voltage VGH. The transistor T42 has a first terminal receiving a gate low voltage VGL, a control terminal receiving the gate signal GX(ny), and a second terminal coupled to the first terminal of the transistor T41. The transistor T43 has a first terminal coupled to
10 the first terminal of the transistor T41, a control terminal receiving the gate signal GX(nx), and a second terminal receiving the gate high voltage VGH. The capacitance C41 is coupled between the first terminal of the transistor T41 and one of the reference voltage Vref and the gate high voltage VGH.

[0066] FIG. 8 is a schematic wiring diagram of a tiled display panel according to an
15 embodiment of the disclosure. Please refer to FIG. 1, FIG. 2A, and FIG. 8. In this embodiment, taking the substrate 101 as an example, multiple clock lines LCX may be disposed in the boundary region 120 (two clock lines LCX are shown here as an example). The clock line LCX spans the boundary region 120 along the first direction D1 and is electrically connected to the light-emitting circuit C_{Tem} to transmit multiple clock signals
20 (such as HC1 and HC2) to the light-emitting circuit C_{Tem} correspondingly. Multiple adjacent light-emitting circuits C_{Tem} may receive the same clock signal (such as HC1 and HC2), that is, adjacent rows of the red LED pixels PDR, the green LED pixels PDG, and the blue LED pixels PDB are lit up simultaneously after completing data writing.

[0067] In the embodiment of the disclosure, the number of clock lines LCX may be

determined according to the design requirements. Further, when the number of clock lines LCX is smaller, the wiring cost of the tiled display panel 100 is lower; on the contrary, when the number of clock lines LCX is larger, the time setting flexibility of the clock signals (such as HC1 and HC2) becomes higher.

5 **[0068]** FIG. 9 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure. Please refer to FIG. 1, FIG. 6, FIG. 8, and FIG. 9. In this embodiment, the light-emitting circuit C_{Tem} takes a light-emitting circuit C_{Temc} as an example, and the light-emitting circuit C_{Temc} is roughly the same as the light-emitting circuit C_{Tema}. The difference lies in that the light-emitting circuit C_{Temc} further includes
10 a transistor T33 (corresponding to an eleventh transistor). The transistor T33 takes the N-type transistor as an example. The transistor T33 has a first terminal receiving one of the clock signals (such as the clock signals HC1 and HC2), a control terminal coupled to the second terminal of the transistor T31, and a second terminal providing (or coupled to) the light-emitting signal EM(n).

15 **[0069]** FIG. 10 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure. Please refer to FIG. 1, FIG. 6, FIG. 9, and FIG. 10. In this embodiment, the light-emitting circuit C_{Tem} takes a light-emitting circuit C_{Temd} as an example, and the light-emitting circuit C_{Temd} is roughly the same as the light-emitting circuit C_{Temc}. The difference lies in that the light-emitting circuit C_{Temc} further includes
20 a capacitance C31 (corresponding to a third capacitance). The capacitance C31 is coupled between the second terminal of the transistor T31 and one of the reference voltage V_{ref} and the gate low level V_{GL}.

[0070] FIG. 11 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure. Please refer to FIG. 1, FIG. 6, FIG. 10, and FIG. 11. In

this embodiment, the light-emitting circuit C_{Tem} takes a light-emitting circuit C_{Teme} as an example, and the light-emitting circuit C_{Teme} is roughly the same as the light-emitting circuit C_{Temd}. The difference lies in that the light-emitting circuit C_{Temd} further includes a transistor T₃₄ (corresponding to a twelfth transistor). The transistor T₃₄ has a first terminal coupled to the second terminal of the transistor T₃₁, a control terminal receiving the gate signal GX(n) (corresponding to a fourth gate signal), and a second terminal receiving the gate low level VGL.

[0071] FIG. 12 is a schematic circuit diagram of a light-emitting circuit according to an embodiment of the disclosure. Please refer to FIG. 1, FIG. 7, FIG. 8, and FIG. 12. In this embodiment, the light-emitting circuit C_{Tem} takes a light-emitting circuit C_{Temf} as an example, and the light-emitting circuit C_{Temf} is roughly the same as the light-emitting circuit C_{Temb}. The difference lies in that the light-emitting circuit C_{Temf} further includes a transistor T₄₄. The transistor T₄₄ takes the P-type transistor as an example. The transistor T₄₄ has a first terminal receiving one of the clock signals (such as the clock signals HC1~HC3), a control terminal coupled to the first terminal of the transistor T₄₁, and a second terminal providing (or coupled to) the light-emitting signal EM(n).

[0072] FIG. 13A is a schematic wiring diagram of a tiled display panel according to an embodiment of the disclosure. Please refer to FIG. 1, FIG. 2A, and FIG. 13A. In this embodiment, taking the substrate 101 as an example, a single light-emitting driving line Lem may be disposed in the boundary region 120 to replace the light-emitting circuit C_{Tem}. The light-emitting driving line Lem spans the boundary region 120 along the first direction D1, receives a light-emitting signal EM_x, and is electrically connected to the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB in the array to transmit the light-emitting signal EM_x simultaneously to all the red LED pixels PDR, the green LED

pixels PDG, and the blue LED pixels PDB in the array. The red LED pixels PDR, the green LED pixels PDG, and the blue LED pixels PDB are lit up simultaneously after completing data writing.

[0073] FIG. 13B is a schematic diagram of driving waveforms of a tiled display panel according to an embodiment of the disclosure. Please refer to FIG. 1, FIG. 2A, FIG. 13A, and FIG. 13B. In this embodiment, the single frame period at least includes a data enable period DataEnable and a vertical blank period Blanking. Moreover, the data enable period DataEnable may be divided into at least a pixel scanning period P_{SN} and a pixel emission period P_{EM}.

[0074] During the pixel scanning period P_{SN}, the liquid crystal pixel PXCX, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB are opened row by row for data writing. Next, after the data is written, the pixel emission period P_{EM} is entered. During the pixel emission period P_{EM}, the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB are lit up simultaneously and multiple times.

Moreover, during the vertical blank period, the tiled display panel 100 may not display images, that is, the tiled display panel 100 may not perform any operations. In other words, the light-emitting signal EM_x may light up the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB simultaneously in the data enable period DataEnable of each frame period.

[0075] In the embodiment of the disclosure, a voltage pulse wave of the light-emitting signal EM_x may be modulated. For example, the voltage pulse wave of the light-emitting signal EM_x may determine the number of voltage pulse waves of the light-emitting signal EM_x in the single pixel emission period P_{EM} according to the gray scale of the frame. For example, when the frame is brighter, the number of voltage pulse waves may be greater;

when the frame is darker, the number of voltage pulse waves may be smaller, which depends on the circuit design, and the embodiment of the disclosure is not limited thereto.

[0076] In the embodiment of the disclosure, the proportions of the pixel scanning period P_{SN} and the pixel emission period P_{EM} to the single frame period may be changed. For example, when the number of voltage pulse waves of the light-emitting signal EMx is small, the time length of the pixel scanning period P_{SN} may be longer; when the number of voltage pulse waves of the light-emitting signal EMx is large, the time length of the pixel scanning period P_{SN} may be shorter, which depends on the circuit design, and the embodiment of the disclosure is not limited thereto.

[0077] FIG. 13C is a schematic diagram of driving waveforms of a tiled display panel according to an embodiment of the disclosure. Please refer to FIG. 1, FIG. 2A, FIG. 13A, and FIG. 13C. In this embodiment, the single frame period at least includes a data enable period $DataEnable$ and a vertical blank period $Blanking$. Moreover, the data enable period $DataEnable$ may be operated as the pixel scanning period P_{SN} , and the vertical blank period $Blanking$ may be operated as a pixel emission period P_{EM}' .

[0078] During the pixel scanning period P_{SN} , the liquid crystal pixel $PXCX$, the red LED pixel PDR , the green LED pixel PDG , and the blue LED pixel PDB are opened row by row for data writing. Next, after the data is written, the pixel emission period P_{EM}' is entered. During the pixel emission period P_{EM}' , the red LED pixel PDR , the green LED pixel PDG , and the blue LED pixel PDB are lit up simultaneously and multiple times. In other words, the light-emitting signal EMx lights up the red LED pixel PDR , the green LED pixel PDG , and the blue LED pixel PDB simultaneously in the vertical blank period $Blanking$ of each frame period.

[0079] FIG. 14 is a schematic wiring diagram of a tiled display panel according to an

embodiment of the disclosure. Please refer to FIG. 1, FIG. 2A, and FIG. 14. In this embodiment, taking the substrate 101 as an example, three light-emitting driving lines Lem may be further disposed in the boundary region 120 to replace the light-emitting circuit CTem. The light-emitting driving line Lem spans the boundary region 120 along the first direction D1 and receives the red light-emitting signal EMR, the green light-emitting signal EMG, and the blue light-emitting signal EMB respectively. The light-emitting driving line Lem (corresponding to a first light-emitting driving line) receiving the red light-emitting signal EMR is electrically connected to the red LED pixel PDR in the array to transmit the red light-emitting signal EMR to all the red LED pixels PDR in the array; the light-emitting driving line Lem (corresponding to a second light-emitting driving line) receiving the green light-emitting signal EMG is electrically connected to the green LED pixel PDG in the array to transmit the green light-emitting signal EMG to all the green LED pixels PDG in the array; moreover, the light-emitting driving line Lem (corresponding to a third light-emitting driving line) receiving the blue light-emitting signal EMG is electrically connected to the blue LED pixel PDB in the array to transmit the blue light-emitting signal EMB to all the blue LED pixels PDB in the array. Furthermore, after the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB complete data writing, the red LED pixel PDR may determine the lighting time length based on the red light-emitting signal EMR (or the voltage pulse wave thereof) and/or the number of lighting times, the green LED pixel PDG may determine the lighting time length and/or the number of lighting times based on the green light-emitting signal EMG (or the voltage pulse wave thereof), and the blue LED pixel PDB may determine the lighting time length and/or the number of lighting times based on the blue light-emitting signal EMG (or the voltage pulse wave thereof).

[0080] FIG. 15 is a schematic wiring diagram of a tiled display panel according to an

embodiment of the disclosure. Please refer to FIG. 1, FIG. 2A, and FIG. 15. In this embodiment, taking the substrate 101 as an example, the light-emitting driving lines Lem may be disposed in the boundary region 120 (two light-emitting driving lines Lem are shown here as an example) to replace the light-emitting circuit CTem. The light-emitting driving line Lem spans the boundary region 120 along the first direction D1 and is electrically connected to the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB in the array to transmit multiple light-emitting signals (such as EM1 and EM2) correspondingly to the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB in the array. The adjacent rows of red LED pixels PDR, green LED pixels PDG, and blue LED pixels PDB may receive the same light-emitting signal (such as EM1 and EM2), that is, the adjacent rows of red LED pixels PDR, green LED pixels PDG, and blue LED pixel PDB write data in groups, and are lit up simultaneously according to the group after completing data writing.

[0081] In the embodiment of the disclosure, the light-emitting driving line Lem may be disposed between the red LED pixel PDR, the green LED pixel PDG, the blue LED pixel PDB, and the tiled boundary Etile, or may be disposed between the red LED pixel PDR, the green LED pixel PDG, and the blue LED pixel PDB, which depends on the circuit design requirements, and the embodiment of the disclosure is not limited thereto.

[0082] In the embodiment of the disclosure, the number of light-emitting driving lines Lem may be determined according to design requirements. Further, when the number of light-emitting driving lines Lem is smaller, the wiring cost of the tiled display panel 100 is lower; on the contrary, when the number of light-emitting driving lines Lem is greater, the flexibility in time setting of the light-emitting signals (such as EM1 and EM2) becomes higher.

[0083] In summary, in the tiled display panel according to the embodiment of the disclosure, the LED pixel may be lit up based on the light-emitting signal of the light-emitting circuit. In this way, the LED pixel may be driven normally, and the seamless tiled effect can be achieved by taking the advantage of the borderless LED pixel. Moreover, the light-emitting signal may be provided for the LED pixel by the light-emitting driving line to drive the LED pixel normally. Alternatively, the light-emitting driving line may be used to replace the light-emitting circuit to transmit the light-emitting signal to drive the LED pixel.

[0084] Although the present disclosure has been disclosed in the above embodiments, it is not intended to limit the present disclosure, and those skilled in the art can make some modifications and refinements without departing from the spirit and scope of the disclosure. Therefore, the scope of the present disclosure is subject to the definition of the scope of the appended claims.

CLAIMS

Claim 1:

A tiled display panel, comprising:

5 a plurality of substrates, wherein each of the plurality of substrates has a display region and at least one boundary region, and the at least one boundary region is respectively located between the display region and a tiled boundary tiled by the plurality of substrates;

a plurality of liquid crystal pixels, arranged in an array in the display region;

a plurality of light-emitting diode (LED) pixels, arranged in an array in the at least one boundary region; and

10 a plurality of light-emitting circuits, arranged in series in the at least one boundary region along a first direction and electrically connected to the plurality of LED pixels to provide a plurality of light-emitting signals for the plurality of LED pixels.

Claim 2:

15 The tiled display panel according to claim 1, wherein the plurality of light-emitting circuits are arranged in series between the plurality of LED pixels and the tiled boundary.

Claim 3:

20 The tiled display panel according to claim 1, further comprising:

a plurality of first gate lines, spanning the display region along the first direction and receiving a plurality of gate signals; and

a plurality of second gate lines, spanning the display region and the at least one boundary region along a second direction perpendicular to the first direction, wherein each

of the plurality of second gate lines is electrically connected to one or part of the plurality of first gate lines, part of the plurality of liquid crystal pixels, and part of the plurality of LED pixels.

5 Claim 4:

The tiled display panel according to claim 3, further comprising:

a plurality of first break over lines, electrically connected to one of the plurality of second gate lines respectively, and extending along the first direction respectively to be electrically connected to a first-level light-emitting circuit and a next-level light-emitting circuit of the plurality of light-emitting circuits.

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Claim 5:

The tiled display panel according to claim 4, wherein a configuration direction of the first-level light-emitting circuit relative to the second gate line electrically connected to each of the plurality of first break over lines is opposite to a configuration direction of the next-level light-emitting circuit relative to the second gate line electrically connected to each of the plurality of first break over lines.

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Claim 6:

20 The tiled display panel according to claim 3, further comprising:

a plurality of second break over lines, electrically connected to one of the plurality of second gate lines respectively, and extending along the first direction to be electrically connected to a first-level light-emitting circuit of the plurality of light-emitting circuits respectively; and

a plurality of third gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of third gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first gate line electrically connected to each of the third gate lines is closer to the at least one boundary region than the first gate line electrically connected to the plurality of adjacent second gate lines.

Claim 7:

The tiled display panel according to claim 3, further comprising:

a plurality of third break over lines, electrically connected to one of the plurality of second gate lines respectively, and extending along the first direction to be electrically connected to a next-level light-emitting circuit of the plurality of light-emitting circuits respectively; and

a plurality of fourth gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of fourth gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first gate line electrically connected to each of the plurality of fourth gate lines is further away from the at least one boundary region than the first gate lines electrically connected to the plurality of adjacent second gate lines.

Claim 8:

The tiled display panel according to claim 3, further comprising:

a plurality of fifth gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of fifth gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first gate line electrically connected to each of the fifth gate lines is closer to the at least one boundary region than the plurality of first gate lines electrically connected to the plurality of adjacent second gate lines; and

a plurality of sixth gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of sixth gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first gate line electrically connected to each of the plurality of sixth gate lines is further away from the at least one boundary region than the plurality of first gate lines electrically connected to the plurality of adjacent second gate lines.

Claim 9:

The tiled display panel according to claim 1, wherein each of the plurality of liquid crystal pixels comprises:

a switch transistor, having a first terminal receiving a pixel data voltage, a control terminal receiving a first gate signal of the plurality of gate signals, and a second terminal;

a first pixel capacitance, coupled between the second terminal of the switch transistor and a first common terminal; and

a second pixel capacitance, coupled between the second terminal of the switch transistor and a second common terminal.

Claim 10:

The tiled display panel according to claim 1, wherein each of the plurality of LED pixels comprises:

- 5 a light-emitting diode (LED), having an anode and a cathode receiving a system low voltage;
- a first transistor, having a first terminal receiving a pixel data voltage, a control terminal receiving a first gate signal of the plurality of gate signals, and a second terminal;
- a second transistor, having a first terminal receiving a system high voltage, a control terminal coupled to the second terminal of the first transistor, and a second terminal;
- 10 a third transistor, having a first terminal coupled to the second terminal of the second transistor, a control terminal receiving a corresponding one of the plurality of light-emitting signals, and a second terminal coupled to the anode of the LED; and
- a first capacitance, coupled between the control terminal of the second transistor
- 15 and the second terminal of the second transistor.

Claim 11:

The tiled display panel according to claim 1, wherein each of the plurality of LED pixels includes:

- 20 an LED, having an anode and a cathode receiving a system low voltage;
- a fourth transistor, having a first terminal receiving a pixel data voltage, a control terminal receiving a first gate signal of the plurality of gate signals, and a second terminal;
- a fifth transistor, having a first terminal, a control terminal coupled to the second terminal of the fourth transistor, and a second terminal;

a second capacitance, coupled between the first terminal of the fifth transistor and the control terminal of the fifth transistor;

a sixth transistor, having a first terminal receiving a reference voltage, a control terminal receiving the first gate signal, and a second terminal coupled to the first terminal
5 of the fifth transistor;

a seventh transistor, having a first terminal receiving a system high voltage, a control terminal receiving a corresponding one of the plurality of light-emitting signals, and a second terminal coupled to the first terminal of the fifth transistor; and

an eighth transistor, having a first terminal coupled to the second terminal of the
10 fifth transistor, a control terminal receiving a corresponding one of the plurality of light-emitting signals, and a second terminal coupled to the anode of the LED.

Claim 12:

The tiled display panel according to claim 1, wherein each of the plurality of
15 light-emitting circuits comprises:

a ninth transistor, having a first terminal receiving a gate high voltage, a control terminal receiving a second gate signal of the plurality of gate signals, and a second terminal coupled to a corresponding one of the plurality of light-emitting signals; and

a tenth transistor, having a first terminal coupled to the second terminal of the
20 ninth transistor, a control terminal receiving a third gate signal of the plurality of gate signals, and a second terminal receiving a gate low level.

Claim 13:

The tiled display panel according to claim 12, wherein each of the plurality of

light-emitting circuits further comprises:

an eleventh transistor, having a first terminal receiving one of a plurality of clock signals, a control terminal coupled to the second terminal of the ninth transistor, and a control terminal coupled to the corresponding one of the plurality of light-emitting signals.

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Claim 14:

The tiled display panel according to claim 12, wherein each of the plurality of light-emitting circuits comprises:

a third capacitance, coupled between the second terminal of the ninth transistor
10 and one of a reference voltage and the gate low level.

Claim 15:

The tiled display panel according to claim 12, wherein each of the plurality of light-emitting circuits comprises:

15 a twelfth transistor, having a first terminal coupled to the second terminal of the ninth transistor, a control terminal receiving a fourth gate signal of the plurality of gate signals, and a second terminal receiving the gate low level.

Claim 16:

20 The tiled display panel according to claim 1, further comprising:

a plurality of clock lines, receiving a plurality of clock signals and electrically connected to the plurality of light-emitting circuits to transmit the plurality of clock signals to the plurality of light-emitting circuits respectively.

Claim 17:

The tiled display panel according to claim 1, wherein a material of the plurality of substrates comprises one of a P-type amorphous silicon (a-Si) substrate, an N-type amorphous silicon (a-Si) substrate, an indium gallium zinc oxide (IGZO) substrate, and a low-temperature polycrystalline silicon (LTPS) substrate.

Claim 18:

The tiled display panel according to claim 1, wherein the plurality of LED pixels comprise a plurality of red LED pixels, a plurality of green LED pixels, and a plurality of blue LED pixels.

Claim 19:

A tiled display pane, comprising:

a plurality of substrates, wherein each of the plurality of substrates has a display region and at least one boundary region, and the at least one boundary region is respectively located between the display region and a tiled boundary tiled by the plurality of substrates;

a plurality of liquid crystal pixels, arranged in an array in the display region;

a plurality of LED pixels, arranged in an array in the at least one boundary region;

and

at least one light-emitting driving line, receiving at least one light-emitting signal, spanning the at least one boundary region along a first direction, and electrically connected to the plurality of LED pixels to provide the at least one light-emitting signal for the plurality of LED pixels.

Claim 20:

The tiled display panel according to claim 19, wherein the at least one light-emitting driving line comprises a light-emitting driving line, the light-emitting driving line receives a light-emitting signal and is electrically connected to the plurality of LED pixels
5 to provide the light-emitting signal for the plurality of LED pixels.

Claim 21:

The tiled display panel according to claim 20, wherein the light-emitting signal
lights up the plurality of LED pixels during a data enable period of a frame period.

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Claim 22:

The tiled display panel according to claim 20, wherein the light-emitting signal
lights up the plurality of LED pixels during a vertical blank period of a frame period.

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Claim 23:

The tiled display panel according to claim 19, wherein the plurality of LED
pixels comprise a plurality of red LED pixels, a plurality of green LED pixels, and a plurality
of blue LED pixels, and the at least one light-emitting driving line comprises a first light-
emitting driving line, a second light-emitting driving line, and a third light-emitting driving
20 line,

the first light-emitting driving line receives a red light-emitting signal and is
electrically connected to the plurality of red LED pixels to provide the red light-emitting
signal for the plurality of red LED pixels,

the second light-emitting driving line receives a green light-emitting signal and

is electrically connected to the plurality of green LED pixels to provide the green light-emitting signal to the plurality of green LED pixels, and

the third light-emitting driving line receives a blue light-emitting signal and is electrically connected to the plurality of blue LED pixels to provide the blue light-emitting
5 signal for the plurality of blue LED pixels.

Claim 24:

The tiled display panel according to claim 19, wherein the at least one light-emitting driving line comprises a plurality of light-emitting driving lines coupled to the
10 plurality of LED pixels to light up the plurality of LED pixels in groups.

Claim 25:

The tiled display panel according to claim 19, wherein the plurality of light-emitting driving lines are disposed between the plurality of LED pixels and the tiled
15 boundary.