

Logarithmic Intermediate-Frequency Amplifier

This invention relates to a logarithmic intermediate-frequency amplifier, and more particularly, to a logarithmic intermediate-frequency amplifier having true logarithmic characteristic or pseudo logarithmic characteristic.

2. Description of the Related Art

In general, a logarithmic intermediate-frequency (IF) amplifier comprises IF amplifiers cascade-connected to each other in a multistage connection manner, rectifiers for receiving output signals of these IF amplifiers in a successive manner, and an adder for adding all output signals of these rectifiers to each other, and is generally formed on a bipolar integrated circuit. This is based on such advantageous facts that bipolar transistor is superior in noise characteristic as well as small in sensitivity degradation when considered from the viewpoint of a received input, and it can be driven even at a low impedance or at a large capacity because the bipolar transistor has a high drivability and the like.

Recently, a C-MOS logarithmic IF amplifier has been demanded to be developed in order to effectively use the advantages of the C-MOS integrated circuit. In this case, however, the following problems have been pointed out on a structural basis:

An MOS transistor is large in $1/f$ noise, so that it is required to have an intermediate-frequency (IF) band cut off its low band side in order to prevent the sensitivity from being degraded from the viewpoint of a received input. So-called HPF (High Pass Filter) characteristic to cut off this low band side can be equivalently obtained by providing IF amplifiers in a multistage cascade-connection manner through coupling capacitors. In this case, however, a coupling capacitor to be inserted is desired to be small in capacity. On the other hand, the multistage connection of the IF amplifiers through the coupling capacitors makes that the rectifiers receiving output signals of respective IF amplifiers differentiate the signal waveforms thereof, thus making it easy to vary the direct-current value of an output of each rectifier. As a result, in order to obtain a good linear logarithmic characteristic, it is unavoidably required to expand the frequency band of an input signal of

each rectifier to the low frequency side, that is, it is required that the capacity of a coupling capacitor to be insertedly used is increased.

Accordingly, in order to practically realize the C-MOS logarithmic IF amplifier, such a problem has been arisen that for the capacity of a coupling capacitor to be used, such contradictory requirements as shown above must be satisfied. In addition, in case that the capacity of a coupling capacitor to be used is increased, there arises a problem on the drivability of the IF amplifier itself as well.

Next, as a pseudo - logarithmic IF amplifier of a polygonal line approximation type formed on a C-MOS integrated circuit, such a circuit as is, for example, shown in Fig. 1 is known conventionally. This circuit is disclosed in the Japanese Laid-Open Patent Application No. 62-292010, which comprises n differential amplifiers respectively including MOS transistor pairs $(T01, T01)$, $(T02, T02)$, ..., and $(T0n, T0n)$ and constant-current sources $I01, I02, \dots$ and $I0n$. These differential amplifiers are cascaded in a n -stage connection manner. The differential amplifiers of the first through n th stages are connected to full-wave

rectifiers comprising two pairs of transistors (T_{11} and T_{1k}), (T_{21} and T_{2k}), ..., and (T_{n1} and T_{nk}), and n constant-current sources I_{11} , I_{12} , ..., and I_{1n} for driving these two pairs of transistors, respectively. The differential amplifier of the $(n+1)$ th stage has a full-wave rectifier comprising two pairs of MOS transistors ($T(n+1)$, and $T(n+1)k$) and two constant-current sources $I_{n(n+1)}$ for driving the two pairs of them, and receiving an output signal of the differential amplifier at the n th stage.

These $2(n+1)$ pairs of transistors (T_{11} and T_{1k}), (T_{21} and T_{2k}), ..., and ($T(n+1)1$ and $T(n+1)k$) forming full-wave rectifiers each has a gate-width (W) and gate-length (L) ratio (W/L) of $1:k$ ($k>1$) thereby to constitute an unbalanced differential pair. Then, in respective two pairs, the transistors having a gate-width (W) and gate-length (L) ratio (W/L) of one (1), or (T_{11} and T_{11}), (T_{21} and T_{21}),, and ($T(n+1)1$ and $T(n+1)1$) have the drains and gates connected respectively in common, and on the other hand, those having the ratio (W/L) of k , or the transistors (T_{1k} and T_{1k}), (T_{2k} and T_{2k}), ..., and ($T(n+1)k$ and $T(n+1)k$) have the drains and gates connected respectively in common.

Next to the $(n+1)$ th stage, an adder comprising three

MOS transistor pairs (T10, T20), (T30, T40) and (T50, T60) is provided, which sums up the outputs of the full-wave rectifiers of the first to the (n+1)th stages.

With the pseudo-logarithmic IF amplifier arranged as above, the operation will be described below.

First, a transconductance parameter α can be expressed in terms of the gate-width and gate-length ratio (W_{11}/L_{11}) of the transistor T11 on the first stage by the following equation (1);

$$\alpha = \mu_n(C_{ox}/2) (W_1/L_1) \dots\dots (1)$$

where, μ_n is a mobility of MOS transistor; and C_{ox} is a gate oxide film capacity per unit area.

In addition, with the transistor pair (T11, T1k) on the first stage, a ratio k between the gate-width and gate-length ratio of one transistor T11 of the pair and that of the other transistor T1k can be expressed as follows;

$$k = \frac{(W_{1k}/L_{1k})}{(W_{11}/L_{11})} \dots\dots (2)$$

Further in addition, in the two pairs of transistors (T11 and T1k) of the first stage, if the gate-to-source voltages of respective transistors are expressed as V_{gs1} , V_{gs2} , V_{gs3} and V_{gs4} , and the threshold voltage of each transistor is expressed as V_t , the currents of respective transistors I_1 , I_2 , I_3 and I_4 can be expressed as follows;

$$I_1 = \alpha (V_{gs1} - V_t)^2 \dots\dots (3)$$

$$I_2 = k\alpha (V_{gs2} - V_t)^2 \dots\dots (4)$$

$$I_3 = \alpha (V_{gs3} - V_t)^2 \dots\dots(5)$$

$$I_4 = k\alpha (V_{gs4} - V_t)^2 \dots\dots (6)$$

Here, these currents I_1 , I_2 , I_3 and I_4 can be expressed in terms of a current I_{11} of the constant-current source of the first stage as follows;

$$I_1 + I_2 = I_{11} \dots\dots (7)$$

$$I_3 + I_4 = I_{11} \dots\dots (8)$$

Also, an input voltage V_{IN} of the two pairs of transistors (T_{11} and T_{1k}) of the first stage can be expressed in terms of the gate-to-source voltages V_{gs1} , V_{gs2} , V_{gs3} and V_{gs4} of the transistors as follows;

$$V_{IN} = V_{gs1} - V_{gs2} = V_{gs4} - V_{gs3} \dots\dots (9)$$

As a result, an output current ΔI_1 of the two pairs of transistors (T_{11} and T_{1k}) can be expressed as follows;

$$\begin{aligned} \Delta I_1 &= (I_1 - I_2) - (I_4 - I_3) \\ &= \frac{-2(1 - 1/k) \{(1 + 1/k) \cdot I_{11} - 2\alpha \cdot V_{IN}^2\}}{(1 + 1/k)^2} \dots\dots (10) \end{aligned}$$

From Eq.(10), it can be found that the output current ΔI_1 has a square full-wave rectification characteristic with respect to the input voltage V_{IN} .

In the same manner as above, an output current ΔI_2 of the two pairs of transistors (T_{21} and T_{2k}) of the second stage $\dots\dots$, and an output current I_{n+1} of the two

pairs of the transistors $T(n+1)1$ and $T(n+1)k$ can be respectively expressed as follows;

$$\Delta I_2 = \frac{-2(1 - 1/k) \{(1 + 1/k) \cdot I_{22} - 2\alpha \cdot V_{IN}^2\}}{(1 + 1/k)^2} \dots\dots(11)$$

$$\Delta I_{n+1} = \frac{-2(1 - 1/k) \{(1 + 1/k) \cdot I(n+1) - 2\alpha \cdot V_{OUT}^2\}}{(1 + 1/k)^2} \dots\dots(12)$$

Here, it is clear that the output currents ΔI_1 , $\Delta I_2 \dots$, ΔI_{n+1} and the constant-current sources I_{11} , I_{22} , $\dots$, and $I_{n(n+1)}$ of respective stages are related as shown by the following equations (13) to (15);

$$-2I_{11} \leq \Delta I_1 \leq 2I_{11} \dots\dots(13)$$

$$-2I_{22} \leq \Delta I_2 \leq 2I_{22} \dots\dots(14)$$

$$-2I_{n+1} \leq \Delta I_{n+1} \leq 2I_{n+1} \dots\dots(15)$$

This means that even if the input voltage V_{IN} and the output voltages $V_1, V_2 \dots, V_{OUT}$ of respective stages are made large, the output currents $\Delta I_1, \Delta I_2 \dots, \Delta I_{n+1}$ are always within the respective ranges shown by Eqs.(13) to (15). In addition, the voltage $V_1, V_2, \dots, V_{OUT}$ are output voltages of the differential amplifiers of respective stages, and as the input voltage V_{IN} is increased gradually, these voltages are successively saturated in the order of $V_{OUT}, \dots V_2$, and V_1 .

Also, the output current I_{OUT} of the adder consisting of the three MOS transistor pairs $(T_{10}, T_{20}), (T_{30}, T_{40})$ and (T_{50}, T_{60}) can be expressed as follows;

$$I_{OUT} = \Delta I_1 + \Delta I_2 + \dots + \Delta I_{n+1} \dots\dots(16)$$

As a result, by suitably setting the constant current values $I_{01}, I_{02}, \dots$, and I_{0n} of the constant-current sources of respective stages and the resistance values $R_{01},$

R_{02} , ..., and R_{0n} of resistors to be connected to the drains of respective transistors, the maximum output voltages of the differential amplifiers of respective stages can be made of a constant sign. This means that the characteristic of the output current I_{OUT} can be made approximately of a logarithmic characteristic to the input voltage V_{IN} .

With the conventional pseudo-logarithmic IF amplifier arranged as shown above, it makes one full-wave rectifier of two unbalanced differential transistor pairs and as a result, the constant-current source is required to be used twice in number as many as the rectifier, resulting in arising such a problem that current consumption unavoidably becomes large. In addition, considering from the viewpoint of the circuit structure, one rectifier uses two unbalanced differential transistor pairs and as a result, the circuit scale disadvantageously becomes large.

This invention was made with a view to solving the above-mentioned problems. an object of this invention is to provide a logarithmic IF amplifier in which contradictory requirements on the capacity of a coupling capacitor to be inserted can be satisfied thereby to be formed on a C-MOS integrated circuit.

Another object of this invention is to provide a pseudo-logarithmic IF amplifier capable of reducing power consumption as well as decreasing circuit scale.

As the applications related to this invention, the followings are concerned; the Japanese Patent Application No. 2-292866 previously made by the same applicant; the U. S. Patent Application No. 784,502 which was made correspondingly thereto; and the British, German and French Patent Application No. 91310038.4 based on the European Patent Convention.

SUMMARY OF THE INVENTION

(1) In a first aspect of this invention, a C-MOS logarithmic IF amplifier is provided which is realizable on a C-MOS integrated circuit.

A C-MOS logarithmic IF amplifier of this aspect comprises a plurality of IF amplifiers cascade-connected through a first coupling capacitor to each other, a plurality of rectifiers each receiving a signal from the corresponding one of the IF amplifiers through a second coupling capacitor different in capacity from the first coupling capacitor, and an adder for adding the output

signals of the rectifiers to each other.

With the C-MOS logarithmic IF amplifier arranged as above, the first and second coupling capacitors are preferable to be connected in series to each other thereby cascade - connecting the IF amplifiers therethrough. The rectifiers each is applied with an output signal of the corresponding one of the IF amplifiers at the connection point of the corresponding first and second coupling capacitors.

An IF amplifier to be used for this invention is not specifically limited in structure thereby, an arbitrarily structured one can be used therefor, and a rectifier to be used for this invention is not specifically limited in structure thereby, so that either of a half-wave or full-wave rectifier can be used therefor.

With the C-MOS logarithmic IF amplifier of this aspect, the IF amplifiers are connected through the first coupling capacitor to each other and the rectifiers are connected to each other through the second coupling capacitor different in capacity from the first coupling capacitor. As a result, by setting the first and second coupling capacitors at optimum capacitive values respectively, the IF amplifiers

each makes it possible to have its frequency band cut off the low band side thereof, and the rectifiers each makes it possible to have its frequency band expanded to the low band side. Accordingly, $(1/f)$ noise of an IF amplifier can be reduced thereby restricting degradation of noise figure (NF). In addition, the input band of a rectifier can be expanded to the low band side thereby obviating excessive signal differentiation and positively maintaining linearity of the logarithmic characteristic. Consequently, the C-MOS logarithmic IF amplifier according to this invention can be realized on a C-MOS integrated circuit.

(2) In a second aspect of this invention, a pseudo-logarithmic IF amplifier is provided which is realizable on a C-MOS integrated circuit. This amplifier has two types, a first and second.

A pseudo-logarithmic IF amplifier of the first type comprises a plurality of differential amplifiers cascade-connected in a plurality of stages, a first half-wave rectifier for receiving an input signal of the differential amplifier of a first one of the stages, a plurality of second half-wave rectifiers each receiving an output signal of the corresponding one of the differential amplifiers

other than that at the first stage, and an adder for adding the direct-current components of outputs of the first and second rectifiers. The first and second rectifiers each has one or more unbalanced differential transistor pairs different in gate-width and gate-length ratio from each other thereby outputting the direct-current component of a differential output current of the same.

A pseudo-logarithmic IF amplifier of the second type comprises a plurality of differential amplifiers cascade-connected in a plurality of stages, a first half-wave rectifier for receiving an input signal of the differential amplifier of a first one of the stages, a plurality of second half-wave rectifiers each receiving an output signal of the corresponding one of the differential amplifiers other than that at the first stage, and an adder for adding outputs of the first and second half-wave rectifiers and outputting the direct-current components thus added, or for receiving outputs of the first and second rectifiers to form their direct-current components thereby to be added to each other. Similar to the first type, the first and second rectifiers each has one or more unbalanced differential transistor-pairs different in gate-width and gate-length

ratio from each other, but different from the first type in that each of them is so structured that is adapted to output its differential output current directly.

With the first and second types of the pseudo-logarithmic IF amplifier in this aspect, in case that two or more unbalanced differential transistor-pairs different in gate-width and gate-length ratio are to be provided, it is preferable that the transistors each with a relatively small gate-width and gate-length ratio have the drains and gates connected respectively in common, and the transistors each with a relatively large gate-width and gate-length ratio have the drains and gates connected respectively in common.

With the pseudo-logarithmic IF amplifier according to this invention, a half-wave rectifier having one or more unbalanced differential transistor-pairs is used as the rectifier, and a direct - current component of its differential output current is added, or its differential output current is added and then, the direct-current component is taken out therefrom. As a result, current consumption and circuit scale can be advantageously reduced.

In addition, when two or more unbalanced differential transistor pairs are provided, an improvement in linearity

of logarithmic characteristic results as compared with the case that one pair of them is used.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing an example of a conventional pseudo-logarithmic IF amplifier.

Fig. 2 is a circuit block diagram of a C-MOS logarithmic IF amplifier according to a first embodiment of this invention.

Fig. 3 is a circuit block diagram of a C-MOS logarithmic IF amplifier according to a second embodiment of this invention.

Fig. 4 is a circuit diagram showing one example of a rectifier to be used in the amplifier shown in Fig. 2 or 3.

Fig. 5 is a circuit diagram showing another example of a rectifier to be used in the amplifier shown in Fig. 2 or 3.

Fig. 6 is a circuit diagram of a pseudo-logarithmic IF amplifier according to a third embodiment of this invention.

Fig. 7 is a characteristic diagram of the amplifier shown in Fig. 6.

Fig. 8 is a circuit diagram of a pseudo-logarithmic IF

amplifier according to a fourth embodiment of this invention.

Fig. 9 is a circuit diagram of a pseudo-logarithmic IF amplifier according to a fifth embodiment of this invention.

Fig. 10 is a circuit diagram of a half-wave rectifier to be used in the amplifier shown in Fig. 9.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of this invention will be described below while referring to Figs. 2 to 10.

[First Embodiment]

Fig. 2 shows a C-MOS logarithmic IF amplifier according to a first embodiment of this invention, in which a plurality of IF amplifiers A1, A2, ... are cascaded in a multistage connection manner in order to amplify an IF signal successively. The multistage cascade - connected amplifiers A1, A2, ... have rectifiers B1, B2, ... connected thereto in order to rectify their output signals, respectively. Output signals of the rectifiers B1, B2, ... are sent to an adder C to be added to each other and outputted. The IF amplifiers A1, A2, ... the rectifiers B1,

B2,... and the adder C are respectively made of MOS transistors.

These IF amplifiers A1, A2, ... are cascade-connected to each other through the two capacitors which are connected in series between each adjacent two of these IF amplifiers. Each of the IF amplifiers A1, A2,... is connected to the corresponding one of these rectifiers B1, B2, ... at the connection point of the two capacitors connected in series therebetween. Namely, the IF amplifiers A1 and A2 are cascade-connected to each other through the capacitors CA1 and CB1 which are disposed in series therebetween. The IF amplifier A1 is connected to the rectifier B1 at the connection point of the capacitors CA1 and CB1. In addition, the IF amplifiers A2 and A3 are cascade-connected to each other through the capacitors CA2 and CB2 which are disposed in series therebetween, and the IF amplifier A2 is connected to the rectifier B2 at the connection point of the capacitors CA2 and CB2. The IF amplifiers A3 and A4, A4 and A5,... are cascade-connected to each other and connected correspondingly to the rectifiers B3, B4,... in the same manner as shown above.

In the following description, an IF amplifier Ai,

rectifier B_i and capacitor CA_i and CB_i ($i = 1, 2, \dots$) typically show there amplifiers, rectifiers and capacitors, respectively. Thus, an input signal to a rectifier B_i is supplied to the gate of a MOS transistor thereof, so that the input impedance becomes high and yet the direct-current biasing to the gate can be made of a high input impedance. As a result, if the input impedance of the rectifier B_i is neglected, a combined capacity C_i of the capacitors CA_i and CB_i can be approximated as follows:

$$C_i = (CA_i CB_i) / (CA_i + CB_i) \dots\dots (21)$$

That is, the IF amplifiers A_i and $A_{(i+1)}$ are coupled through the combined capacity C_i to each other, and the IF amplifier A_i and the rectifier B_i are coupled to each other through only the capacity of the capacitor CA_i .

In addition, the low band side of a frequency band is determined by the differential characteristic (HPF characteristic) of each coupling capacitor. As a result, the ratio of a low band side cut-off frequency fc_{IFI} of the IF amplifier A_i and a low band side cut-off frequency fc_{RECTi} of the rectifier B_i can be expressed as follows;

$$f_{cIFI}/f_{cRECTi} \cong C_{Ai}/C_i = (C_{Ai}/C_{Bi}) + 1 (>1) \dots\dots (22)$$

From Eq.(22), it can be found that the low band side cut-off frequency f_{cIFI} of the IF amplifier A_i can be made high compared with the low band side cut-off frequency f_{cRECTi} of the rectifier B_i .

In this case, a load capacity of the IF amplifier A_i is the combined capacity C_i , however, if $C_{Ai} = C_{Bi} = C_o$, from Eq.(21), $C_i = (1/2) C_o$, which means that the capacity of an inter-stage coupling capacitor of the IF amplifier A_i becomes half that of a coupling capacitor with the rectifier B_i . As a result, from Eq.(22), $f_{cIFI} = 2f_{cRECTi}$ is obtained, which means that the low band side cut-off frequency of the rectifier B_i can be decreased up to a half of that of the IF amplifier A_i .

Consequently, according to this invention, an IF amplifier is allowed the low band side of its frequency band to be cut off and on the other hand, a rectifier is allowed its frequency band to be expanded to the low band side, so that a logarithmic IF amplifier can be obtained which is formed on a C-MOS integrated circuit without arising any

important problem.

[Second Embodiment]

Fig. 3 shows a C-MOS logarithmic IF amplifier according to a second embodiment of this invention. In Fig. 3, an IF amplifier A_i is connected through a capacitor C_{Bi} to an IF amplifier $A_{(i+1)}$ and through a capacitor C_{Bi} whose capacity is different from that of the capacitor C_{Ai} to a rectifier B_i . Other components are arranged as explained in the first embodiment. The C-MOS logarithmic IF amplifier of this embodiment makes it possible to obtain the same effects as shown in the first embodiment.

[First Example of Rectifier to be used in First and Second Embodiments]

In the first and second embodiments, any circuit made of C-MOS transistor can be arbitrarily used as the rectifier B_i . In this case, however, a squaring circuit can be pointed out as an example as shown in Fig. 4, which is disclosed in the Japanese Laid-Open Patent Application No. 63-24377 made by the same one as the inventor of this amplifier, thus being used as a squaring full-wave rectifier.

In Fig. 4, the squaring circuit comprises a first differential transistor-pair consisting of a MOS transistor T1 with a gate-width and gate-length ratio ($W1/L1$) and a MOS transistor T2 with a gate-width and gate-length ratio ($W2/L2$) and a second differential transistor-pair consisting of a MOS transistor T3 with the same ratio as that of the transistor T1, ($W1/L1$), and a MOS transistor T4 with the same ratio as that of the transistor T2, ($W2/L2$). In this case, if the ratio ($W1/L1$) is made one (1), the ratio ($W2/L2$) is made k. The transistors T1 and T2 have the sources connected in common and the transistors T3 and T4 have the sources connected in common, which are connected through their connection points to constant-current sources I0, respectively. The gate of the transistor T1 is connected to that of the transistor 4, and the gate of the transistor T2 is connected to that of the transistor T3. The collector of the transistor T1 is connected to that of the transistor T3, and the collector of the transistor 2 is connected to that of the collector T4. An input voltage VIN is applied across the common gate of the transistors T1 and T4 and the common gate of the transistors T2 and T3, which are different in the gate-width and gate-length ratio from each

other. Transistors T5 and T6 each is the primary side transistor of a current mirror circuit. A subtracting circuit S subtracts a current flowing in the output line of the second differential pair from a current flowing in the output line of the first differential pair. VDD is a voltage source.

With the circuit arranged as above, the characteristics will be explained below.

Drain currents I_{d1} and I_{d2} of the transistors T1 and T2 of the first differential pair and drain currents I_{d3} and I_{d4} of the transistors T3 and T4 of the second differential pair can be expressed as follows;

$$I_{d1} = \alpha_1 (V_{GS1} - V_T)^2 \dots\dots (23)$$

$$I_{d2} = \alpha_1 \cdot k (V_{GS2} - V_T)^2 \dots\dots (24)$$

$$I_{d3} = \alpha_1 (V_{GS3} - V_T)^2 \dots\dots (25)$$

$$I_{d4} = \alpha_1 \cdot k_1 (V_{GS4} - V_T)^2 \dots\dots (26)$$

where, V_{GS1} , V_{GS2} , V_{GS3} and V_{GS4} are gate-to-source voltages

of the transistors T1, T2, T3 and T4, respectively, and V_T is the threshold voltage of each transistor.

In these equations, if the mobility of an electron of MOS transistor is expressed as μ_n and the gate oxide film capacity per unit area of MOS transistor is expressed as C_{ox} , the following equations can be obtained, as

$$\alpha_1 = \mu_n(C_{ox}/2) (W_1/L_1) \dots\dots (27)$$

$$k_1 = (W_2/L_2)/(W_1/L_1) \dots\dots(28)$$

In addition, the constant-current value I_0 of the constant-current source, and the input voltage V_{IN} can be expressed as follows;

$$I_{d1} + I_{d2} = I_0 \dots\dots (29)$$

$$I_{d3} + I_{d4} = I_0 \dots\dots (30)$$

$$V_{GS1} - V_{GS2} = V_{IN} \dots\dots (31)$$

$$V_{GS3} - V_{GS4} = V_{IN} \dots\dots(32)$$

Here, if ΔIdI is defined as

$$\Delta IdI = Id1 - Id2 \dots\dots(33).$$

it can be obtained by the following equation, as

$$\begin{aligned} \Delta IdI = & [-(1+1/k1) (1-1/k1)I0 + 2\alpha 1 \cdot (1+1/K1) \cdot VIN^2 + \\ & 4\alpha 1 \cdot VIN \cdot (1/K1^{1/2}) \cdot \{(1+1/K1)(I0/\alpha 1) - VIN^2\}^{1/2}] / (1+1/k1)^2 \\ & \dots\dots (34). \end{aligned}$$

In addition, if $\Delta IdII$ is defined as

$$\Delta IdII = Id3 - Id4 \dots\dots(35),$$

it can be obtained as follows;

$$\begin{aligned} \Delta IdII = & [(1+1/k1) (1-1/k1)I0 + 2\alpha 1 \cdot (1-1/K1)VIN^2 + \\ & 4\alpha 1 \cdot VIN (1/K1^{1/2}) \{(1+1/K1)(I0/\alpha 1) - VIN^2\}^{1/2}] / (1+1/k1)^2 \\ & \dots\dots(36) \end{aligned}$$

Hence,

$$\Delta Id = \Delta IdI - \Delta IdII$$

$$= [-2(1+1/k_1) (1-1/k_1)I_0 + 4\alpha_1 \cdot (1-1/K_1)V_{IN}^2]/(1+1/k_1)^2 \dots\dots\dots(37)$$

From Eq.(37), it can be found that the current difference ΔI_d includes the square term of the input voltage V_{IN} .

In the other hand, the current difference ΔI_d can be expressed as follows;

$$\Delta I_d = (I_{d1} + I_{d3}) - (I_{d2} + I_{d4}) \dots\dots\dots(38)$$

From Eq.(38), it can be found that such an output current that is expressed by Eq.(37) including the square term of the input voltage V_{IN} can be obtained by the subtracting circuit S.

As explained above, the square characteristic can be obtained with a simple circuit arranged as shown in Fig. 4, which comprises two differential pairs each consisting of two transistors different in the gate-width and gate-length ratio (W/L) from each other, and in which the transistors with the same gate-width and gate-length ratio (W/L) have the drains connected in common to each other and yet, their outputs become opposite in phase.

[Second Example of Rectifier to be used in First and Second Embodiments]

Another example of a squaring circuit to be used in these embodiments is shown in Fig. 5, which comprises four MOS transistors. In Fig. 5, MOS transistors M1 and M2 constitute a first differential transistor-pair to be driven by a constant-current source I0, and MOS transistors M3 and M4 constitute a second differential transistor-pair to be driven by a constant-current source obtained by the following equation;

$$\{2 \cdot k_2^{1/2} / (k_2 + 1)\} \cdot I_0 \quad \dots\dots(39)$$

Further in Fig. 5, the drain of the transistor M1 is connected to that of the transistor M3, and the drain of the transistor M2 is connected to that of the transistor M4. The gate of the transistor M1 is connected to that of the transistor M4, and the gate of the transistor M2 is connected to that of the transistor M3.

Here, with the first differential pair, if the gate-width (W1) and gate-length (L1) ratio (W1/L1) of the transistor M1 is made one (1), the gate-width (W2) and gate-

length (L2) ratio (W2/L2) of the transistor M2 is k2. That is, Eq.(28) can be satisfied between them.

Referring to the second differential pair, the gate-width (W3) and gate-length (L3) ratio (W3/L3) of the transistor M3 is equal to the gate-width (W4) and gate-length (L4) ratio (W4/L4) of the transistor M4, which can be expressed in terms of k2 as follows:

$$(W3/L3) = (W4/L4) = \{4k2 \cdot k2^{1/2} / (k2+1)\}^2 \dots\dots (40)$$

As a result, the drain currents Id1' and Id2' of the transistors M1 and M2 of the first differential pair can be respectively expressed as follows; where VGS1' and VGS2' show the gate-to-source voltage of the transistors M1 and M2 respectively.

$$Id1' = \mu n(COX/2) (W1/L1) (VGS1'-VT)^2 \dots\dots (41)$$

$$Id2' = \mu n(COX/2) k(W1/L1) (VGS2'-VT)^2 \dots\dots(42)$$

In addition, the constant-current I0 and the input voltage VIN can be respectively obtained as follows;

$$I_{d1}' + I_{d2}' = I_0 \dots\dots (43)$$

$$V_{GS1}' - V_{GS2}' = V_{IN} \dots\dots (44)$$

Here, if the difference of the I_{d1}' and I_{d2}' is expressed as I_{dP} , or

$$\Delta I_{dP} = I_{d1}' - I_{d2}' \dots\dots (45),$$

it can be obtained as follows;

$$\Delta I_{dP} = \frac{-(1-1/k_2) \cdot \{(1+1/k_2)I_0 - 2\alpha^2 \cdot V_{IN}^2\} + 4\alpha^2 \{(1+1/k_2)(I_0/\alpha^2) - V_{IN}^2\}^{1/2}}{(1+1/k_2)^2} \dots\dots (46)$$

Similarly, the drain currents I_{d3}' and I_{d4}' of the transistors M3 and M4 can be respectively expressed as follows;

$$Id3' = \{4k2 \cdot k2^{1/2}/(k2 + 1)^2\} \cdot \alpha 2 (VGS3' - VT)^2 \dots\dots (47)$$

$$Id4' = \{4k2 \cdot k2^{1/2}/(k+1)^2\} \cdot \alpha 2 (VGS4' - VT)^2 \dots\dots (48)$$

In addition, the constant-current and the input voltage can be respectively expressed as follows:

$$Id3' + Id4' = \{2 \cdot k2^{1/2}/(k2 + 1)\} \cdot I0 \dots\dots (49)$$

$$VGS4' - VGS3' = VIN \dots\dots (50)$$

Here, if the difference of the $Id3'$ and $Id4'$ is expressed as IdQ , or

$$\Delta IdQ = Id3' - Id4' \dots\dots (51),$$

it can be obtained as follows:

$$\begin{aligned} \Delta IdQ &= \{-4 \cdot k2^{1/2}/(2k + 1)^2\} \alpha 2 \cdot VIN \\ &\times \left[\{4 \cdot k2^{1/2} \cdot I0/(k2+1)\} \cdot \{(k2+1)^2/4k2 \cdot k2^{1/2} \cdot \alpha 2\} - VIN^2 \right]^{1/2} \\ &= -\{4 \alpha 2 \cdot (1/k2^{1/2})/(k2+1)^2\} \cdot VIN \\ &\times \left[\{4 \cdot k2^{1/2} \cdot I0/(k2+1)\} \cdot \{(k2+1)^2/4k2 \cdot k2^{1/2} \cdot \alpha 2\} - VIN^2 \right]^{1/2} \end{aligned}$$

.....(52)

As a result, the differential output current I can be obtained as follows;

$$\Delta I = I_1 - I_2 = I_{dP} - I_{dQ}$$

$$= \frac{(1-1/k_2) \cdot \{2\alpha^2 \cdot V_{IN}^2 - (1+1/k_2) \cdot I_0\}}{(1 - 1/k_2)^2}$$

$$= \{2k_2(k_2-1)\alpha^2/(k_2+1)^2\} \cdot V_{IN}^2 - \{(k_2-1)/(k_2+1)\} \cdot I_0$$

.....(53)

From Eq.(53), it can be found that such a differential output current ΔI that is proportional to the square of the input voltage V_{IN} can be obtained.

As explained above, the squaring circuit comprises two differential pairs each consisting of two transistors whose gate-width and gate-length ratios are optimized thereby making a differential input, so that the squaring circuit is not dependent on variation in threshold voltage due to the forming dispersion of transistors.

[Third Embodiment]

Fig. 6 shows a pseudo - logarithmic IF amplifier according to a third embodiment of this invention, which comprises n differential amplifier $A1'$, $A2'$, ..., and A_n' which are cascaded in a n -stage connection manner. a first half-wave rectifier for receiving an input signal to the differential amplifier $A1'$ of the first stage, n second half-wave rectifiers respectively receiving output signals of the differential amplifiers $A1'$, $A2'$, ..., and A_n' from the first to n th stages, and an adder for adding the output signals of these half-wave rectifiers. The differential amplifiers $A1'$, $A2'$, ..., and A_n' are of the same in characteristic. and yet, the first and n second half-wave rectifiers are of the same in structure.

The first stage half-wave rectifier comprises an unbalanced differential transistor - pair consisting of n -channel MOS transistors $M11$ and $M12$ different in gate-width and gate-length ratio from each other, a current mirror circuit consisting of p -channel MOS transistors $M13$ and $M14$ for forming a differential current, a capacitor $C01$ for erasing an alternating current component from the differential current thus formed. and a constant-current

source I01, thus outputting the direct-current component of the differential output current. The capacitor C01 is provided between the drains of the transistors M11 and M12, and the constant-current source I01 is provided between their sources connected in common and the ground. The drains of the transistors M13 and M14 connected in common are applied with a source voltage VDD. An input voltage VIN to the differential amplifier A1' is applied between the gates of the transistors M11 and M12. A direct-current component $\overline{\Delta I_1}$ of the differential output current is applied between the gate of a MOS transistor M10 and that of a MOS transistor M20 of the adder.

The second half-wave rectifier of the second stage has the same structure as that of the first one, and comprises an unbalanced differential transistor-pair consisting of transistors M21 and M22 different in gate-width and gate-length ratio from each other, a current mirror circuit consisting of transistors M23 and M24 for forming a differential current, a capacitor C02 for erasing an alternating current component of the differential current thus formed, and a constant-current source I02, thus outputting the direct-current component of the differential

output current. The capacitor C02 is provided between the drains of the transistors M21 and M22, and the constant-current source I02 is provided between their sources connected in common and the ground. The drains of the transistors M23 and M24 connected in common are applied with the source voltage VDD. An output voltage V1 of the differential amplifier A1' is applied between the gates of the transistors M21 and M22. A direct-current component $\overline{\Delta I_2}$ of the differential output current is applied between the gates of the MOS transistors M10 and M20 of the adder.

The second half-wave rectifier of the (n+1)th stage has the same arrangement as above. That is, it comprises an unbalanced differential transistor pair consisting of transistors M(n+1)1 and M(n+1)2 different in gate-width and gate-length ratio from each other, a current mirror circuit consisting of transistors M(n+1)3 and M(n+1)4 for forming a differential current, a capacitor C0(n+1) for erasing an alternating current component from the differential current thus formed, and a constant-current source I0(n+1), thus outputting the direct-current component of the differential output current. The capacitor C0(n+1) is provided between the drains of the transistors M(n+1)1 and M(n+1)2, and the

constant-current source $I_0(n+1)$ is provided between their sources connected in common and the ground. The drains of the transistors $M(n+1)3$ and $M(n+1)4$ connected in common are applied with the source voltage V_{DD} . An output voltage V_{OUT} of the differential amplifier A_n is applied between the gates of the transistors $M(n+1)1$ and $M(n+1)2$. A direct-current component $\overline{\Delta I_{n+1}}$ of the differential output current is applied between the gates of the MOS transistors $M10$ and $M20$ of the adder.

With the transistor pairs $(M11, M12)$, $(M21, M22)$, ..., and $(M(n+1)1, M(n+1)2)$ respectively forming the unbalanced differential-pairs as described above, the gate-width and gate-length ratio of each of the transistors $M11$, $M21$, ..., and $M(n+1)1$ is smaller than that of each of the transistors $M12$, $M22$, ..., and $M(n+1)2$.

The adder comprises a current mirror circuit consisting of a differential-pair of p channel MOS transistors $M10$ and $M20$, thereby adding the output currents of $(n+1)$ half-wave rectifiers, or the direct-current components $\overline{\Delta I_1}$, $\overline{\Delta I_2}$, ..., and $\overline{\Delta I_{n+1}}$ outputted from respective half-wave rectifiers.

In this case, the unbalanced differential transistor-

pairs of respective half-wave rectifiers are not necessary to have a gate-width and gate-length ratio equal to each other, however, it is made equal to each other in this explanation for the simplification purpose. Thus, the transconductance parameter α_3 can be expressed in terms of the gate-width and gate-length ratio (W_{11}/L_{11}) of the transistor M_{11} as follows;

$$\alpha_3 = \mu_n(C_{ox}/2) (W_{11}/L_{11}) \dots\dots (61)$$

In addition, in one unbalanced differential pair, the ratio k_3 between the gate-width and gate-length ratios of the transistors forming the pair can be typically expressed in terms of the ratios (W_{11}/L_{11}) and (W_{12}/L_{12}) of the transistors M_{11} and M_{12} of the first stage as follows;

$$k_3 = (W_{12}/L_{12})/(W_{11}/L_{11}) \dots\dots (62)$$

As a result, drain currents I_{d11} and I_{d12} of the transistors M_{11} and M_{12} can be expressed as follows, respectively;

$$I_{d11} = \alpha_3 (V_{GS11} - V_t)^2 \dots\dots(63)$$

$$I_{d12} = k_3 \cdot \alpha_3 (V_{GS12} - V_t)^2 \dots\dots(64)$$

In addition, the constant current I_{01} and input voltage V_{IN} can be expressed as follows, respectively;

$$I_{d11} + I_{d12} = I_{01} \dots\dots(65)$$

$$V_{GS11} - V_{GS12} = V_{IN} \dots\dots(66)$$

From the equations, $\Delta I_1 (= I_{d11} - I_{d12})$ can be obtained as follows:

$$\begin{aligned} \Delta I_1 &= I_{d11} - I_{d12} \\ &= \frac{-\left(1 + \frac{1}{k_3}\right) \left\{ \left(1 + \frac{1}{k_3}\right) I_{01} - 2 \alpha_3 V_{IN}^2 \right\} + 4 \alpha_3 \frac{V_{IN}}{k_3^{1/2}} \left\{ \left(1 + \frac{1}{k_3}\right) \frac{I_{01}}{\alpha_3} V_{IN}^2 \right\}^{1/2}}{\left(1 + \frac{1}{k_3}\right)^2} \end{aligned} \dots\dots(67)$$

Thus, if I_1 is defined as shown by the following

equation (68), a direct-current component ΔI_{1DC} , a square characteristic component ΔI_{1SQ} and an alternating current component ΔI_{1DIFF} can be expressed as follows, respectively;

$$\Delta I_1 = I_{1DC} + I_{1SQ} + I_{1DIFF} \dots \dots (68)$$

$$\Delta I_{1DC} = \{-(K_3-1)/(k_3+1)\} \cdot I_{01} \dots \dots (69)$$

$$\Delta I_{1SQ} = \{2k_3(k_3-1) \alpha^3 / (k_3+1)^2\} \cdot V_{IN}^2 \dots \dots (70)$$

$$\Delta I_{1DIFF} = \frac{4 \alpha^3 \cdot k_3 \cdot V_{IN} \left\{ \frac{(k_3+1) I_{01}}{\alpha^3} - k_3 \cdot V_{IN}^2 \right\}^{1/2}}{(k_3 + 1)^2} \dots \dots (71)$$

From these equations, the I_{1DIFF} may be considered to be a direct-current characteristic of generally so-called balanced differential - pair that is approximately proportional to the input voltage V_{IN} , thus becoming the alternating current component to be erased by the capacitor C_{01} . As a result, the direct-current component $\overline{\Delta I_1}$ of ΔI_1

becomes the sum of ΔI_{1DC} and a direct-current component $\overline{\Delta I_{1SQ}}$ of the ΔI_{1SQ} as shown by the following equation (72), and if the input voltage V_{IN} is supposed to be of a sine wave and expressed as the following equation (73), the direct-current component $\overline{\Delta I_1}$ can be obtained by the following equation (74):

$$\overline{\Delta I_1} = \Delta I_{1DC} + \overline{\Delta I_{1SQ}} \quad \dots\dots (72)$$

$$V_{IN} = V_{IN}(t) = |V_{IN}| \cos(2\pi ft) \quad \dots\dots (73)$$

$$\overline{\Delta I_1} = \frac{k_3 - 1}{k_3 + 1} I_{O1} + \frac{k_3(k_3 - 1) \alpha_{3-11}}{(k_3 + 1)^2} |V_{IN}|^2 \quad \dots\dots (74)$$

In the same manner as above, the direct-current component $\overline{\Delta I_2}$ of the output current ΔI_2 of the second stage unbalanced differential transistor-pair (M_{21} , M_{22}), and the direct-current component $\overline{\Delta I(n+1)}$ of the output current $\Delta I(n+1)$ of the final stage differential transistor-pair ($M(n+1)1$, $M(n+1)2$) can be obtained as follows; respectively;

$$\overline{\Delta I_2} = \frac{k_3 - 1}{k_3 + 1} I_{02} + \frac{k_3(k_3-1) \cdot \alpha_3}{(k_3 + 1)^2} |V_{IN}|^2 \dots\dots\dots (75)$$

$$\overline{\Delta I_{n+1}} = \frac{k_3 - 1}{k_3 + 1} I_{0(n+1)} + \frac{k_3(k_3-1) \cdot \alpha_3}{(k_3 + 1)^2} |V_{OUT}|^2 \dots\dots\dots (76)$$

As a result, the outputs, or the direct - current components of the half-wave rectifiers from the first to (n+1)th stages are added to each other by the adder which is the current mirror circuit consisting of MOS transistors M10 and M20 in pair, thus obtaining an output current IRSSI as follows:

$$IRSSI = \overline{\Delta I_1} + \overline{\Delta I_2} + \dots\dots\dots + \overline{\Delta I_{n+1}} \dots\dots\dots (77)$$

As a result, the output voltage VRSSI can be obtained as follows: where RRSSI is a load resistance.

$$\begin{aligned} VRSSI &= RRSSI \cdot IRSSI \\ &= RSSI \cdot (\overline{\Delta I_1} + \overline{\Delta I_2} + \dots\dots\dots + \overline{\Delta I_{n+1}}) \dots\dots\dots (78) \end{aligned}$$

Accordingly, with the circuit shown in Fig. 6, as the

input voltage V_{IN} is increased gradually, the output voltages V_1 , V_2 , ..., and V_{OUT} of the differential amplifiers A_1' , A_2' , ..., and A_n' are successively saturated in the order from V_{OUT} to V_1 , which is characteristically shown on a decibel (dB) unit basis in Fig. 7.

[Fourth Embodiments]

As clear from the above explanations with the third embodiment, the pseudo - logarithmic IF amplifier may have a capacitor disposed on the adder side thereof. As a result, the half-wave rectifiers and the adder may be arranged, for example, as follows;

Fig. 8 shows an fourth embodiment of this invention. In the pseudo logarithmic IF amplifier in Fig. 8, the half-wave rectifier each comprises one unbalanced differential transistor-pair, thereby directly outputting a differential output current. The adder has a current mirror circuit consisting of p-channel MOS transistors M_{30} and M_{40} for forming a differential current and a capacitor C_0 for erasing an alternating current component from the differential current thereby to form the direct-current component and added. The capacitor C_0 is arranged between

the gates connected in common of the p - channel MOS transistors M10 and M20 and the drain of the transistor M20. The other arrangement is same as the third embodiment.

In this embodiment, the half-wave rectifier each comprises one unbalanced differential transistor-pair, so that the amplifier of this embodiment is largely effective to make the circuit scale small.

[Fifth Embodiment]

Fig. 9 shows an fifth embodiment of this invention. In the pseudo - logarithmic IF amplifier in Fig. 9, the capacitor C0 is arranged between the output terminal and the ground. The other arrangement is same as the fourth embodiment.

Thus, the adder may have the capacitor C0 disposed on the output side thereof. In this case, the direct-current component is taken out after adding all the differential currents. This circuit is also largely effective to make the circuit scale small.

[Example of Rectifier to be used in Third to Fifth Embodiments]

With the above-described half-wave rectifiers, each can be formed of at least one unbalanced differential transistor-pair. Here, a rectifier with two unbalanced differential transistor-pair is exemplified in Fig.10, which is obtained by connecting the unbalanced differential transistor-pair (M11, M12) of the third embodiment shown in Fig. 6 and an unbalanced differential transistor-pair (M15, M16) in parallel. The unbalanced differential transistor-pairs (M11, M12) and (M15, M16) are respectively driven by different constant-current sources I_{01} and I_{01}' from each other. The transistors M11 and M15 each with a small gate-width and gate-length ratio have the drains and gates connected in common, and the transistors M12 and M16 each with a large gate-width and gate-length ratio have the drains and gate connected in common.

For the unbalanced differential transistor-pair (M15, M16), the output current thereof ΔI_{12} and the direct-current component thereof $\overline{\Delta I_{12}}$, can be expressed, as in Eqs. (67) and (74), as follows;

$$\Delta I_{12} = I_{d15} - I_{d16}$$

$$= \frac{-(1 - \frac{1}{k_4}) \{ (1 + \frac{1}{k_4}) I_{O1} - 2 \alpha_4 V_{IN}^2 \} + 4 \alpha_4 \frac{V_{IN}}{k_4^{1/2}} \{ (1 + \frac{1}{k_4}) \frac{I_{O1}}{\alpha_4} V_{IN}^2 \}^{1/2}}{(1 + \frac{1}{k_4})^2}$$

..... (81)

$$\Delta I_{12} = \frac{k_4 - 1}{k_4 + 1} I_{O1} + \frac{k_4(k_4 - 1) \alpha_4}{(k_4 + 1)^2} |V_{IN}|^2 \quad \text{..... (82)}$$

Here, in Eqs.(81) and (82), it is supposed that α_2 is equal to α_1 , or $\alpha_4 = \alpha_3$. In this case, the differential amplifiers to be cascade-connected to each other are not required to have the same gain, however, if they have the same gain g_v for simplifying explanations, the following equation will be obtained:

$$\left\{ \frac{k_3 (k_3 - 1)}{(k_3 + 1)^2} \right\} / \left\{ \frac{k_4 (k_4 - 1)}{(k_4 + 1)^2} \right\} = g_v^{1/2} (>1) \quad \text{..... (83)}$$

As a result, Eq.(74) can be expressed as follows:

$$\overline{\Delta I I} = \frac{k_3 - 1}{k_3 + 1} I_{01} + \frac{k_4(k_4 - 1) \alpha_1}{(k_4 + 1)^2} \{g_v |V_{IN}|^2\} \dots\dots (84)$$

Thus, if G_v is defined as shown by the following equation (85) and the input voltage V_{IN} is expressed on a decibel (dB) unit basis, it can be found from these equations that the direct-current component $\overline{\Delta I I}$ of the output current $\Delta I I$ is shifted to operate by $(1/2)G_v$ in the direction that the input level becomes low with respect to the direct-current component $\overline{\Delta I I_2}$ of the output current $\Delta I I_2$:

$$G_v = 20 \log (g_v) \dots\dots (85)$$

This means that for two unbalanced differential transistor-pairs to be disposed at and after the second stage, the same results can be obtained, so that the operational dynamic range of each unbalanced differential transistor-pair will become $(1/2)G_v$, resulting in an improvement in linearity of the logarithmic characteristic thereof.

On the other hand, if the gain g_v of a differential

amplifier A_i is expressed as follows;

$$\left\{ \frac{k_4 (k_4 - 1)}{(k_4 + 1)^2} \right\} / \left\{ \frac{k_3 (k_3 - 1)}{(k_3 + 1)^2} \right\} = g_v^{1/2} \quad (>1) \quad \dots\dots (86)$$

Eq.(82) can be expressed as follows;

$$\overline{\Delta I_{12}} = -\frac{k_4 - 1}{k_4 + 1} I_{01} + \frac{k_3 (k_3 - 1) \alpha 1}{(k_3 + 1)^2} \{g_v |V_{IN}|^2\} \quad \dots\dots (87)$$

This means that when the input voltage V_{IN} is expressed on a decibel (dB) unit basis, the direct-current component $\overline{\Delta I_1}$ of the output current ΔI_1 is shifted to operate by $(1/2)G_v$ in the direction that the input level becomes high with respect to the direct-current component $\overline{\Delta I_{12}}$ of the output current ΔI_{12} . As a result, for any unbalanced differential transistor-pair to be disposed at and after the second stage, the same results can be obtained, so that the operational dynamic range of each unbalanced differential transistor-pair will become $(1/2)G_v$, resulting in an improvement in linearity of the logarithmic characteristic thereof.

In addition, if $n = m$, and the following equations (88) and (89) are satisfied, the operational dynamic range of each unbalanced differential transistor-pair will become $(1/m)Gv$, resulting in an improvement in linearity of the logarithmic characteristic thereof.

$$\left\{ \frac{km-1(km-1-1)}{(km-1+1)^2} \right\} / \left\{ \frac{km(km-1)}{(km+1)^2} \right\} = gv^{1/m} \quad \dots\dots(88)$$

$$\left\{ \frac{km(km-1)}{(km+1)^2} \right\} / \left\{ \frac{km-1(km-1-1)}{(km-1+1)^2} \right\} = gv^{1/m} \quad \dots\dots(89)$$

As explained above, a pseudo-logarithmic IF amplifier of this invention makes it possible to reduce current consumption as well as to decrease the circuit scale. In addition, in case that the half-wave rectifiers each is formed of two or more unbalanced differential transistor-pairs, the logarithmic characteristic can be effectively improved in linearity.

Claims:



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1. A C-MOS logarithmic intermediate - frequency amplifier comprising:

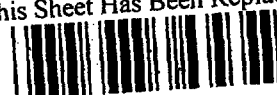
a plurality of intermediate - frequency amplifiers cascade-connected through a first coupling capacitor to each other;

a plurality of rectifiers each receiving a signal from the corresponding one of said plurality of intermediate-frequency amplifiers through a second coupling capacitor different in capacity from said first coupling capacitor; and

an adder for adding output signals of said plurality of rectifiers to each other.

2. A C-MOS logarithmic intermediate-frequency amplifier as claimed in claim 1, wherein said first and second capacitors are connected in series and said plurality of intermediate-frequency amplifiers are cascade-connected through said first and second capacitors thus connected in series.

3. A pseudo-logarithmic intermediate-frequency amplifier





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comprising:

a plurality of differential amplifiers cascade-connected with a plurality of stages;

a first half-wave rectifier receiving an input signal to the differential amplifier of a first one of said plurality of stages;

a plurality of second half-wave rectifiers each receiving an output signal of the corresponding one of said plurality of differential amplifiers other than that of the first stage; and

an adder for adding the direct-current components of output currents of said first and second rectifiers to each other;

Wherein said first and second half-wave rectifiers each has at least one unbalanced differential transistor-pair different in gate-width and gate-length ratio from each other thereby outputting the direct-current component of a differential output current of said at least one unbalanced differential transistor pair.

4. A pseudo-logarithmic intermediate-frequency amplifier as claimed in claim 3. wherein said rectifiers each includes





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at least two said unbalanced differential transistor-pairs, and the transistors of respective pairs each with a relatively small gate-width and gate-length ratio have the drains and gates connected in common and the transistors of respective pairs each with a relatively large gate-width and gate-length ratio have the drains and gates connected in common.

5. A pseudo-logarithmic intermediate-frequency amplifier comprising:

- a plurality of differential amplifiers cascade-connected with a plurality of stages;

- a first half-wave rectifier receiving an input signal of the differential amplifier of a first one of said plurality of stages;

- a plurality of second half-wave rectifiers each receiving an output signal of the corresponding one of said plurality of differential amplifiers other than that of the first stage; and

- an adder for adding output signals of said first and second rectifiers and outputting the direct - current component of a resultant thus obtained;





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wherein said first and second half-wave rectifiers each has at least one unbalanced differential transistor-pair different in gate-width and gate-length ratio from each other thereby outputting differential output current of said at least one unbalanced differential transistor pair.

6. A pseudo-logarithmic intermediate-frequency amplifier as claimed in claim 5, wherein said rectifiers each includes at least two said unbalanced differential transistor-pairs, and the transistors of respective pairs each with a relatively small gate-width and gate-length ratio have the drains and gates connected in common and the transistors of respective pairs each with a relatively large gate-width and gate-length ratio have the drains and gates connected in common.

7. A pseudo-logarithmic intermediate-frequency amplifier comprising:

a plurality of differential amplifiers cascade-connected in a plurality of stages;

a first half-wave rectifier receiving an input signal of the differential amplifier of a first one of said

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plurality of stages;

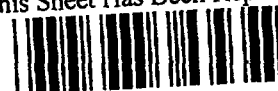
a plurality of second half-wave rectifiers each receiving an output signal of the corresponding one of said plurality of differential amplifiers other than that of the first stage; and

an adder for receiving output currents of said first and second rectifiers to form their direct - current components thereby to be added to each other;

wherein said first and second half-wave rectifiers each has at least one unbalanced differential transistor-pair different in gate-width and gate-length ratio from each other thereby outputting differential output current of said at least one unbalanced differential transistor pair.

8. A pseudo-logarithmic intermediate-frequency amplifier as claimed in claim 7, wherein said rectifiers each includes at least two said unbalanced differential transistor-pairs, and the transistors of respective pairs each with a relatively small gate-width and gate-length ratio have the drains and gates connected in common and the transistors of respective pairs each with a relatively large gate-width and gate-length ratio have the drains and gates connected in common.

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Logarithmic Intermediate-Frequency Amplifier

A C-MOS logarithmic IF amplifier is provided which comprises a plurality of IF amplifiers cascade-connected to each other through a first coupling capacitor, a plurality of rectifiers each receiving a signal from the corresponding one of the plurality of IF amplifiers through a second coupling capacitor different in capacity from the first coupling capacitor, and an adder for adding the output signals of these rectifiers to each other. The first and second coupling capacitors are preferable to be connected in series to cascade-connect those IF amplifiers therethrough. Each of the rectifiers is applied with an output signal of the corresponding one of the IF amplifier from the connection point of the corresponding first and second coupling capacitors. By setting the first and second capacitors at optimum capacitive values, respectively, the IF amplifiers each makes it possible to cut off the low band side of its frequency band and the rectifiers each makes it possible to expand its frequency band to the low band side.



FIG. 1

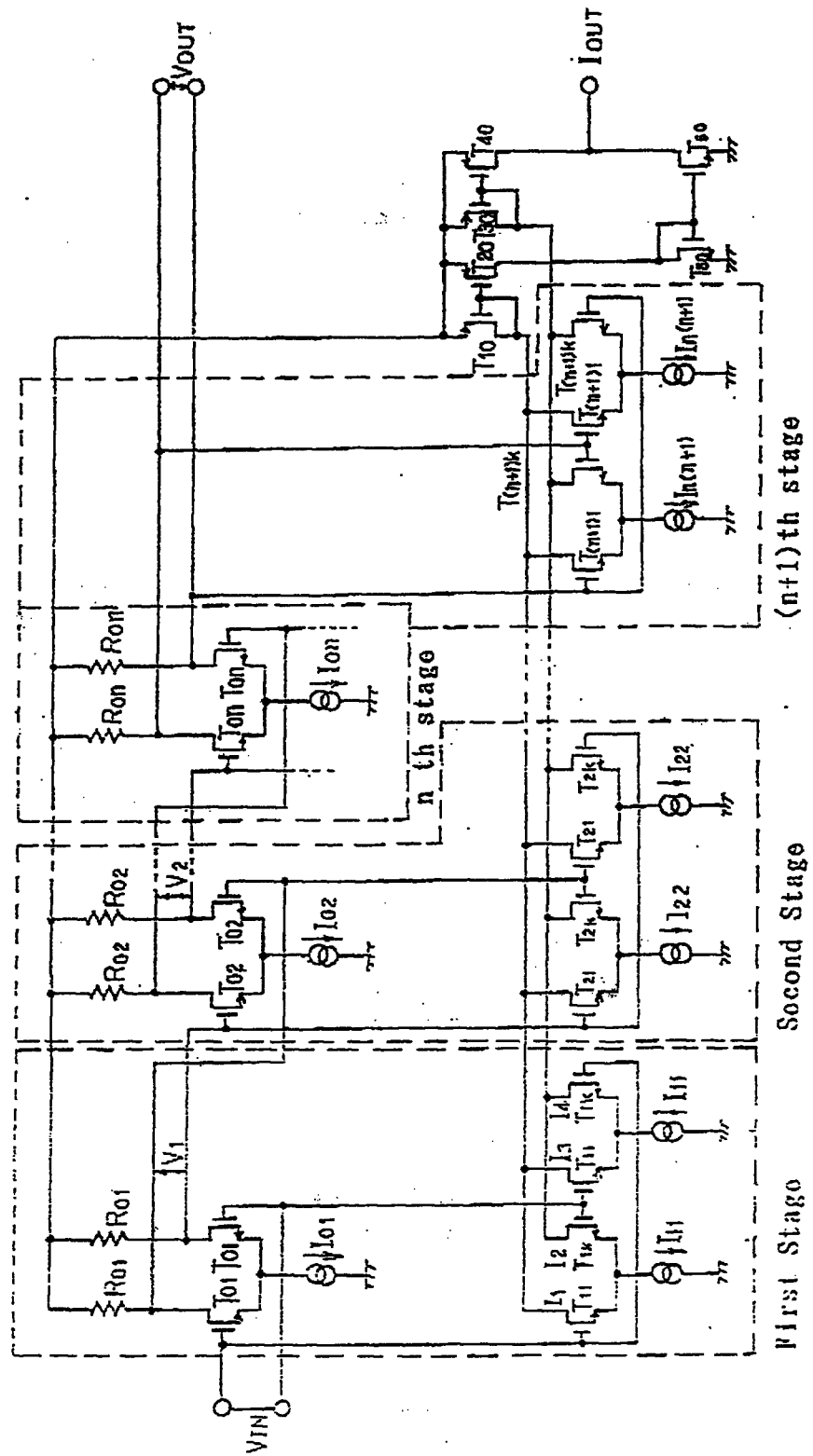


FIG. 2

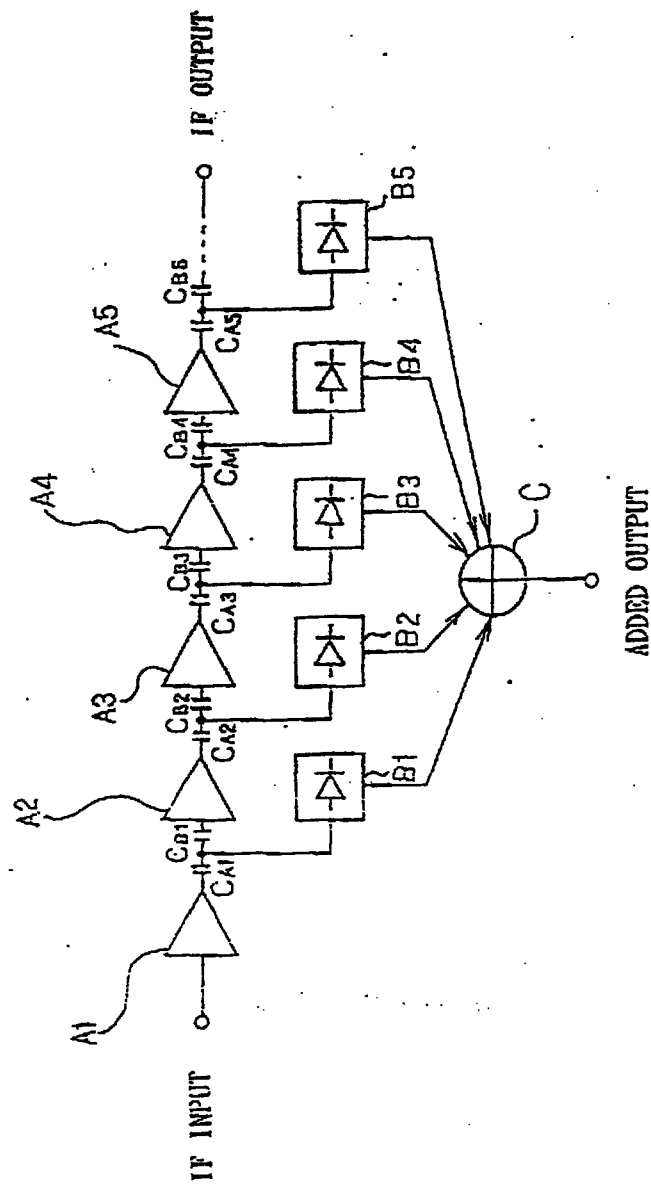


FIG. 3

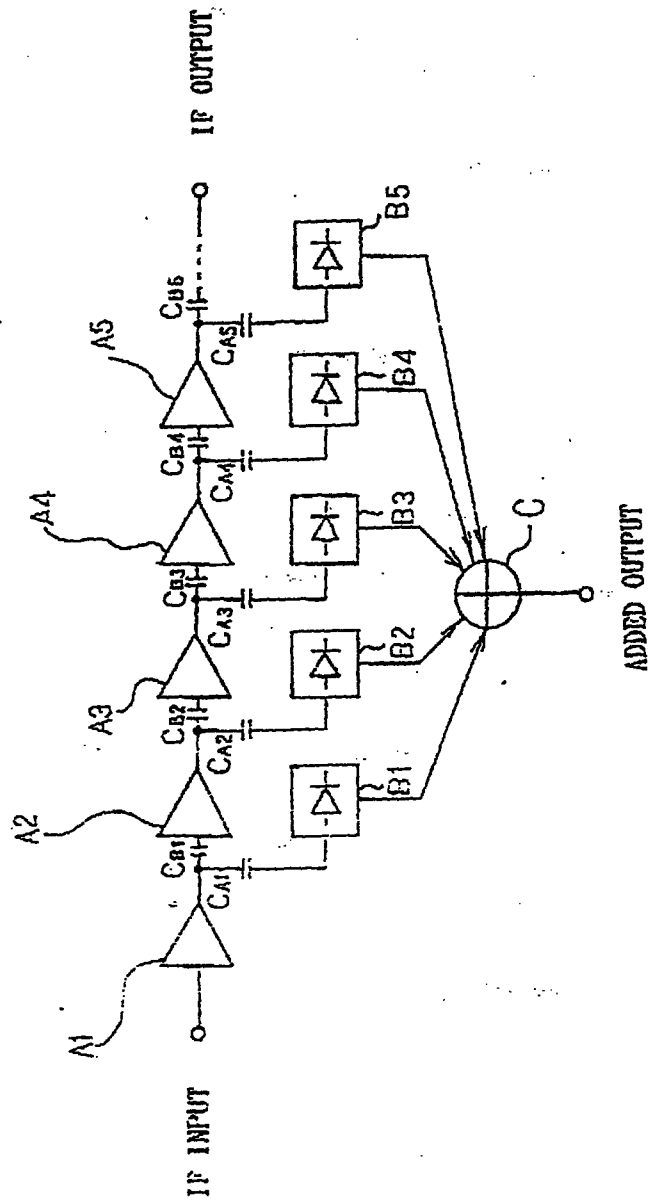


FIG. 4

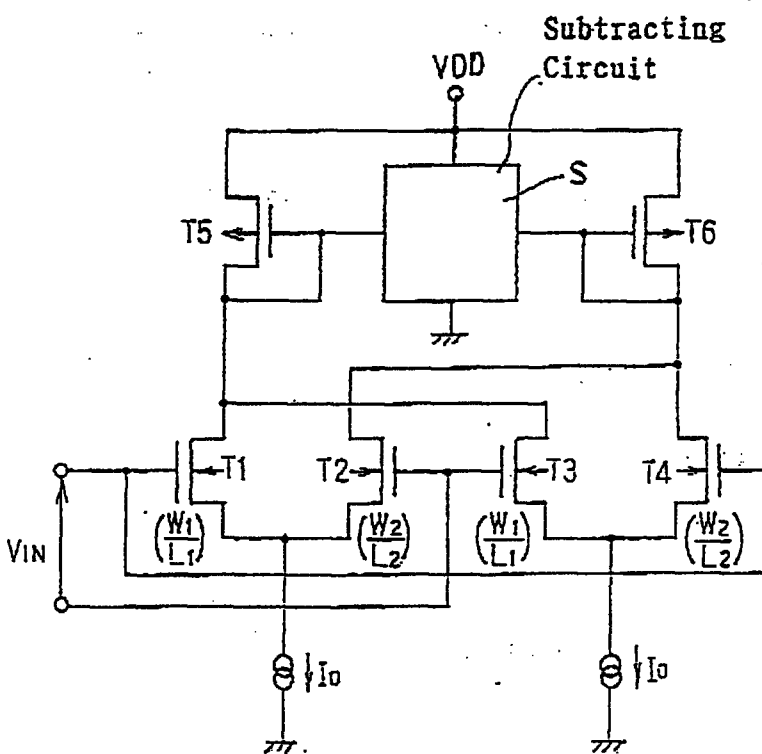


FIG. 5

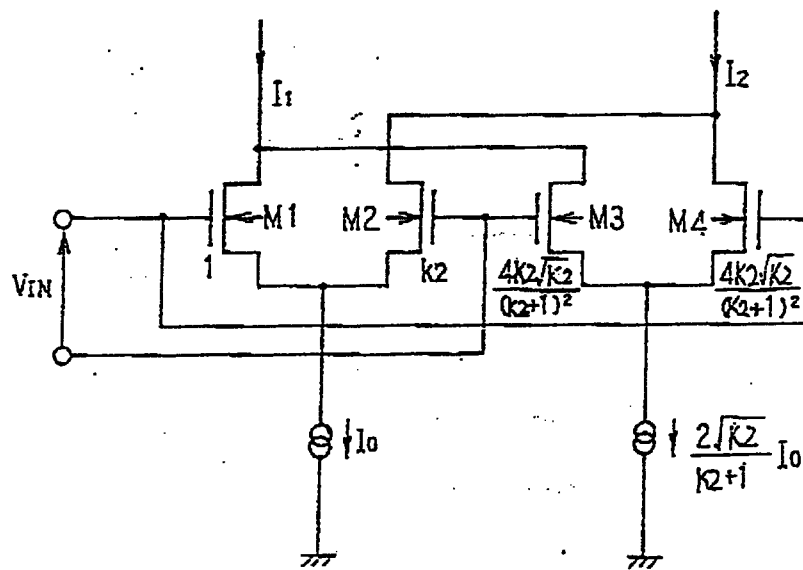


FIG. 6

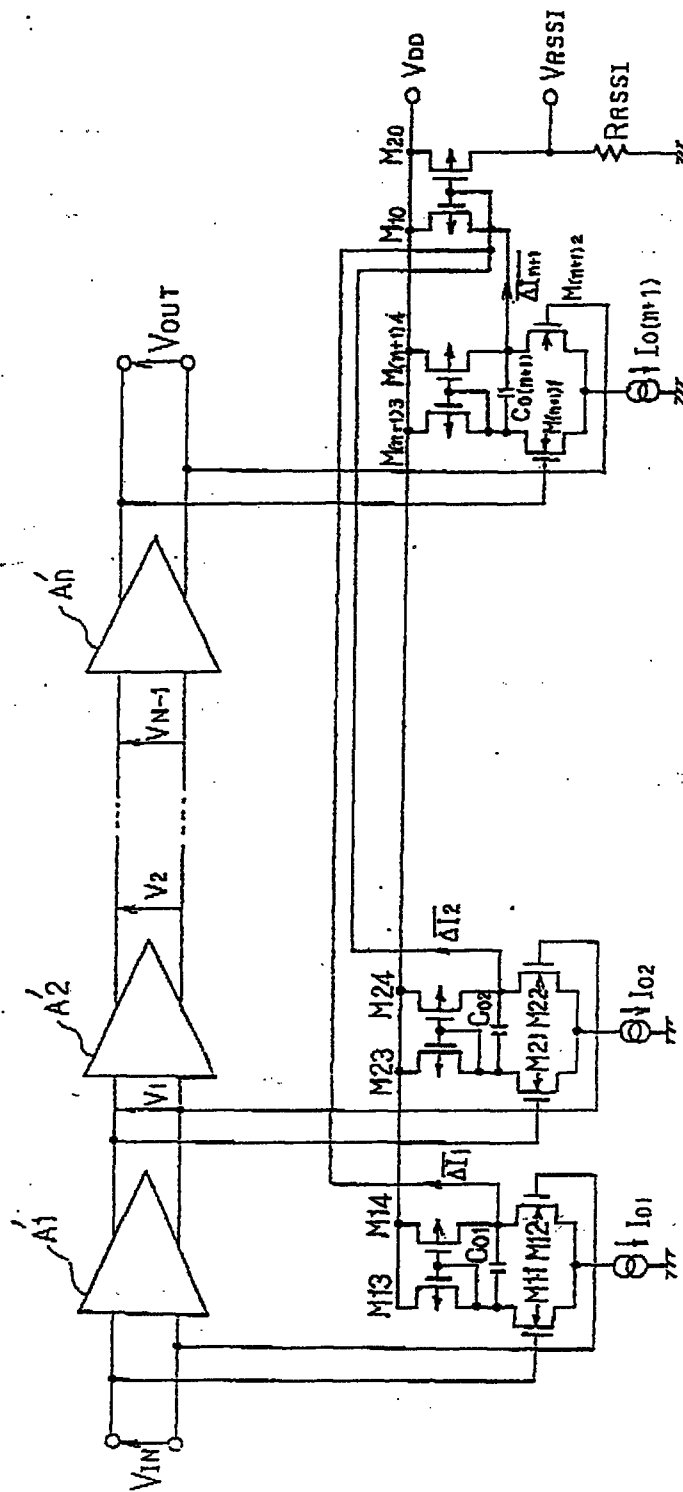


FIG. 7

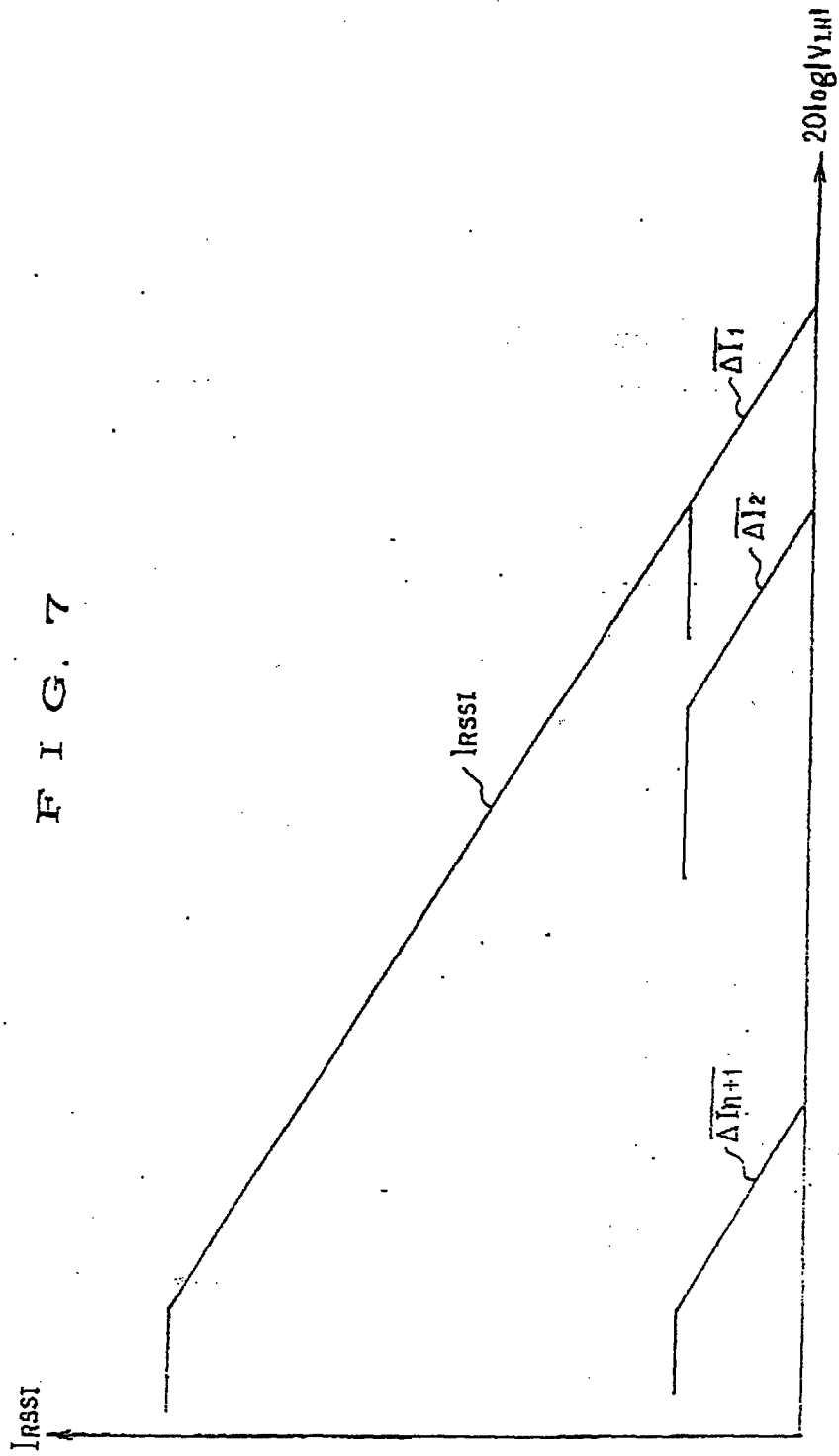


FIG. 8

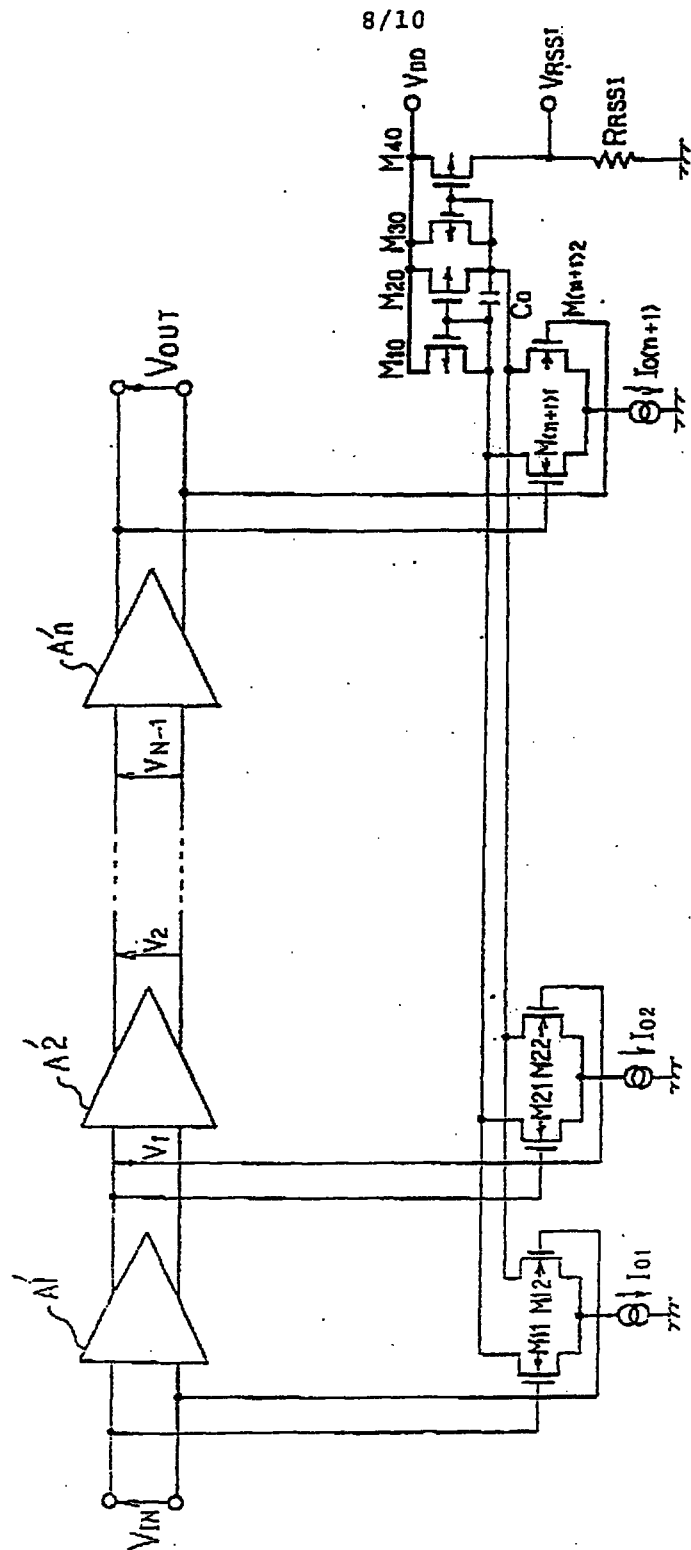


FIG. 9

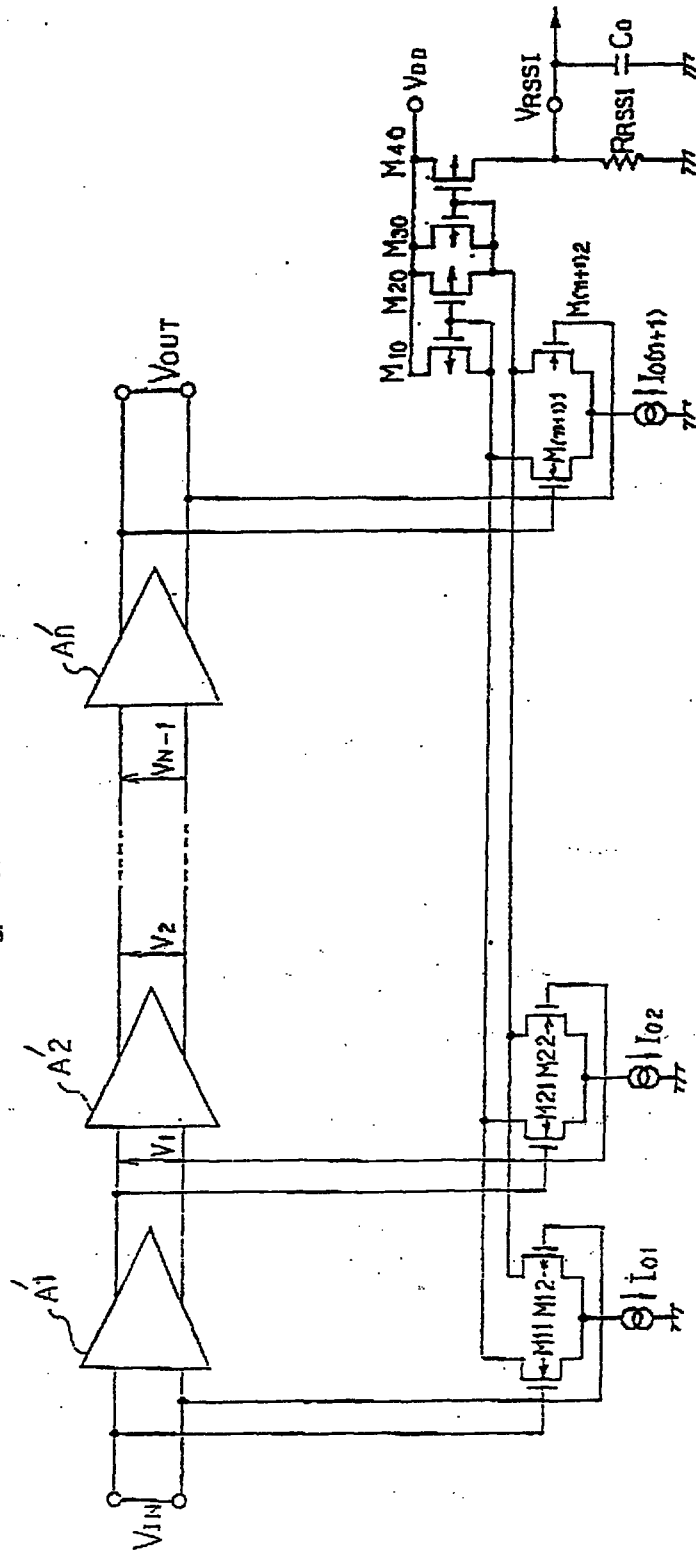
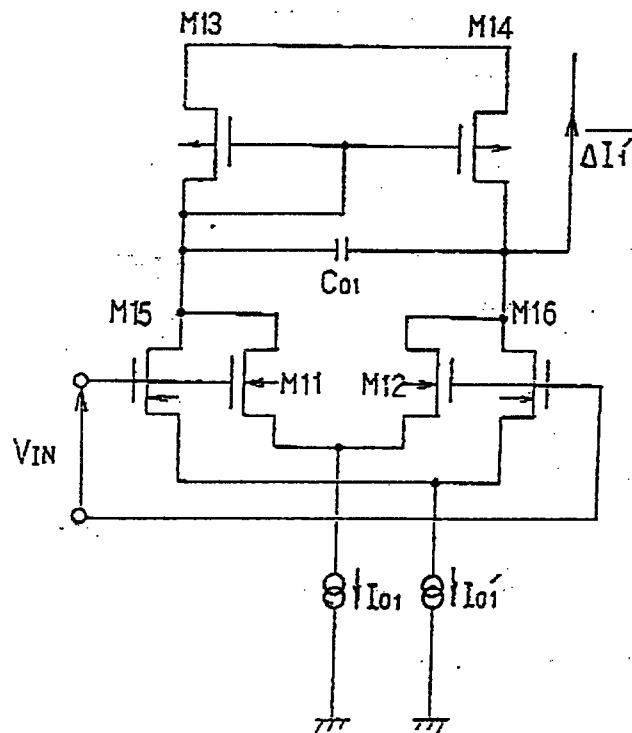


FIG. 10



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ABSTRACT

Logarithmic Intermediate-Frequency Amplifier

A C-MOS logarithmic IF amplifier is provided which comprises a plurality of IF amplifiers cascade-connected to each other through a first coupling capacitor, a plurality of rectifiers each receiving a signal from the corresponding one of the plurality of IF amplifiers through a second coupling capacitor different in capacity from the first coupling capacitor, and an adder for adding the output signals of these rectifiers to each other. The first and second coupling capacitors are preferable to be connected in series to cascade-connect those IF amplifiers therethrough. Each of the rectifiers is applied with an output signal of the corresponding one of the IF amplifier from the connection point of the corresponding first and second coupling capacitors. By setting the first and second capacitors at optimum capacitive values, respectively, the IF amplifiers each makes it possible to cut off the low band side of its frequency band and the rectifiers each makes it possible to expand its frequency band to the low band side.

Fig. 2

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Another object of this invention is to provide a pseudo-logarithmic IF amplifier capable of reducing power consumption as well as decreasing circuit scale.

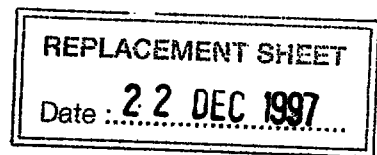
As the applications related to this invention, the followings are concerned; the Japanese Patent Application No. 2-292866 previously made by the same applicant; the US Patent Application No. 784,502 which was made correspondingly thereto; and the British, German and French Patent Application No. 91310038.4 based on the European Patent Convention.

SUMMARY OF THE INVENTION

It is an object of the present invention to ameliorate one or more disadvantages of the prior art.

According to one aspect of the present invention there is provided a C-MOS logarithmic intermediate-frequency amplifier comprising: a plurality of intermediate-

frequency amplifiers cascade-connected, each of said amplifiers being connected through a first coupling capacitor to each other, an intermediate-frequency input signal being applied to one of said amplifiers disposed at a first stage, each of said amplifiers being formed of MOS transistors; a plurality of rectifiers, each of which being connected through a second coupling capacitor to corresponding one of said amplifiers to rectify an output signal from said corresponding one of said amplifiers, each of said rectifiers being formed of MOS transistors; and an adder connected to said rectifiers, said adder receiving output signals of said plurality of rectifiers and adding them to each other, said adder generating an output signal varying substantially logarithmically as a function of said intermediate-frequency input signal applied to said amplifier at said first stage; wherein capacitance values of said first coupling capacitors are set so that each of said amplifiers has a frequency band whose low band side is cut off to reduce



(1/f) noise thereof, and capacitance values of said second coupling capacitors are set so that each of said rectifiers has a frequency band whose low band side is expanded to improve linearity of a logarithmic characteristic of said logarithmic intermediate-frequency amplifier.

According to another aspect of the present invention there is provided a C-MOS logarithmic intermediate-frequency amplifier comprising: a plurality of intermediate-frequency amplifiers cascade-connected, each of said amplifiers being connected through serially connected first and second coupling capacitors to each other, an intermediate-frequency input signal being applied to one of said amplifiers disposed at a first stage; each of said amplifiers being formed of MOS transistors; a plurality of rectifiers, each of which being connected through said first coupling capacitor to a corresponding one of said amplifiers to rectify an output signal from said corresponding

one of said amplifiers; each of said rectifiers being formed of MOS transistors; and an adder connected to said rectifiers, said adder receiving output signals of said plurality of rectifiers and adding them to each other, said adder generating an output signal varying substantially logarithmically as a function of said intermediate-frequency input signal applied to said amplifier at said first stage; wherein capacitance values of said first coupling capacitors are set so that each of said rectifiers has a frequency band whose low band side is expanded to improve linearity of a logarithmic characteristic of said logarithmic intermediate-frequency amplifier, and a combined capacitance value of each of said serially connected first and second capacitors is set so that each of said amplifiers has a frequency band whose low band side is cut off to reduce $(1/f)$ noise of said amplifiers.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing an example of a conventional pseudo-logarithmic IF amplifier.

Fig. 2 is a circuit block diagram of a C-MOS logarithmic IF amplifier according to a first embodiment of this invention.

Fig. 3 is a circuit block diagram of a C-MOS logarithmic IF amplifier according to a second embodiment of this invention.

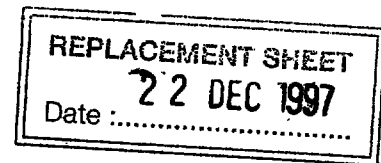
Fig. 4 is a circuit diagram showing one example of a rectifier to be used in the amplifier shown in Figure 2 or 3.

Fig. 5 is a circuit diagram showing another example of a rectifier to be used in the amplifier shown in Figure 2 or 3.

Fig. 6 is a circuit diagram of a pseudo-logarithmic IF amplifier according to a third embodiment of this invention.

Fig. 7 is a characteristic diagram of the amplifier shown in Figure 6.

Fig. 8 is a circuit diagram of a pseudo-logarithmic IF



CLAIMS

1. A C-MOS logarithmic intermediate-frequency amplifier comprising:

a plurality of intermediate-frequency amplifiers cascade-connected, each of said amplifiers being connected through a first coupling capacitor to each other, an intermediate-frequency input signal being applied to one of said amplifiers disposed at a first stage, each of said amplifiers being formed of MOS transistors;

a plurality of rectifiers, each of which being connected through a second coupling capacitor to corresponding one of said amplifiers to rectify an output signal from said corresponding one of said amplifiers, each of said rectifiers being formed of MOS transistors; and

an adder connected to said rectifiers, said adder receiving output signals of said plurality of rectifiers and adding them to each other, said adder generating an output signal varying substantially logarithmically as a function of said intermediate-frequency input signal applied to said amplifier at said first stage;

wherein capacitance values of said first coupling capacitors are set so that each of said amplifiers has a frequency band whose low band side is cut off to reduce (1/f) noise thereof, and capacitance values of said second coupling capacitors are set so that each of said rectifiers has a frequency band whose low band side is expanded to improve linearity of a logarithmic characteristic of said logarithmic intermediate-frequency amplifier.

2. A C-MOS logarithmic intermediate-frequency amplifier comprising:

a plurality of intermediate-frequency amplifiers cascade-connected, each of said amplifiers being connected through serially connected first and second coupling capacitors to each other, an intermediate-frequency input signal being applied to one of said amplifiers disposed at a first stage;

each of said amplifiers being formed of MOS transistors;

a plurality of rectifiers, each of which being connected through said first coupling capacitor to a corresponding one of said amplifiers to rectify an output signal from said corresponding one of said amplifiers;

each of said rectifiers being formed of MOS transistors; and

an adder connected to said rectifiers, said adder receiving output signals of said plurality of rectifiers and adding them to each other, said adder generating an output signal varying substantially logarithmically as a function of said intermediate-frequency input signal applied to said amplifier at said first stage;

wherein capacitance values of said first coupling capacitors are set so that each of said rectifiers has a frequency band whose low band side is expanded to improve linearity of a logarithmic characteristic of said logarithmic intermediate-frequency amplifier, and a combined capacitance value of each of said serially connected first and



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second capacitors is set so that each of said amplifiers has a frequency band whose low band side is cut off to reduce (1/f) noise of said amplifiers.

3. A C-MOS logarithmic intermediate-frequency amplifier as claimed in claim 1, wherein

each of said plurality of rectifiers contains at least one of unbalanced differential pair of MOS transistors, and

said MOS transistors are different in gate-width to gate-length ratios from each other and sources of said transistors are coupled together.

4. A C-MOS logarithmic intermediate-frequency amplifier as claimed in claim 1, wherein each of said plurality of rectifiers comprises a first differential pair of first and second MOS transistors driven by a first constant current source, and a second differential pair of third and fourth MOS transistors driven by a second constant current source,

said second transistor is K times in gate-width to gate-length ratio as much as said first MOS transistor,

said third and fourth MOS transistors are both $\{(4K K^{1/2})/(K+1)^2\}$ times in gate-width to gate-length ratio as much as said first MOS transistor, and

said second constant current source is $\{(2K^{1/2})/(K+1)\}$ times in current value as much as said first constant current source.

5. A C-MOS logarithmic intermediate-frequency amplifier as claimed in claim 2, wherein

each of said plurality of rectifiers contains at least one unbalanced differential pair of MOS transistors, and

said MOS transistors are different in gate-width to gate-length ratios from each other and sources of said transistors are coupled together.

6. A C-MOS logarithmic intermediate-frequency amplifier as claimed in claim 2, wherein each of said plurality of rectifiers comprises a first differential pair of first and second MOS transistors driven by a first constant current source, and a second differential pair of third and fourth MOS transistors driven by a second constant current source,

said second MOS transistor having K times a gate-width to gate-length ratio as said first transistor,

said third and fourth MOS transistors both having $\{(4K-K^{1/2})/(K+1)^2\}$ times the gate-width to gate-length ratio as said first transistor, and

said second constant current source having a current value which is $\{2K^{1/2}/(K+1)\}$ times that of said first constant current source.

ABSTRACT

Logarithmic Intermediate-Frequency Amplifier

A C-MOS logarithmic IF amplifier is provided which comprises a plurality of IF amplifiers cascade-connected to each other through a first coupling capacitor, a plurality of rectifiers each receiving a signal from the corresponding one of the plurality of IF amplifiers through a second coupling capacitor different in capacity from the first coupling capacitor, and an adder for adding the output signals of these rectifiers to each other. The first and second coupling capacitors are preferable to be connected in series to cascade-connect those IF amplifiers therethrough. Each of the rectifiers is applied with an output signal of the corresponding one of the IF amplifier from the connection point of the corresponding first and second coupling capacitors. By setting the first and second capacitors at optimum capacitive values, respectively, the IF amplifiers each makes it possible to cut off the low band side of its frequency band and the rectifiers each makes it possible to expand its frequency band to the low band side.