METHOD OF FABRICATION OF HIGHLY HEAT DISSIPATIVE SUBSTRATES

The invention relates to a method for fabricating composite structures having high heat dissipation properties, dedicated to be substrates for the crystal growth of single-crystal layers aimed to receive electronic devices or components or, substrates including such single-crystal layers.

These structures may especially be useful for dissipating the heat generated by the said components during operation.

They are particularly useful when said components generate a lot of thermal energy, as for high power frequency components (typically more than 900 MHz). Indeed, if the temperature of the single-crystal layer is greater than a threshold temperature, the components could be disturbed or even damaged.

To overcome this drawback, the single-crystal layers are typically made of a nitride semiconductor material having better charge carrying properties (high saturation rate of carriers at high voltages, high breakdown voltages, etc.) than materials such as AsGa. This is particularly true for HEMT (High Electron Mobility Transistor) type components.

To form this type of nitride semiconductor layers, growth substrates made of single-crystal bulk SiC, bulk <111> silicon or bulk sapphire (Al_2O_3) are used.

However, the thermal impedances of <111> Si and sapphire are too high for some high power frequency applications that require greater dissipation of released heat. Thus the components could still be disturbed or damaged.

And single-crystal bulk SiC is a costly material, although it is a reference material in terms of heat dissipation.

Thus there is a need for a substrate which dissipates sufficiently the thermal energy at low cost.

To this aim, US 6,328,796 and US 2003/0064735 disclose the manufacturing of composite structures using a wafer bonding technique comprising the following steps:

- providing a substrate and a wafer with a top single-crystal layer thereon,

- forming a bonding oxide layer on the substrate and/or on the top layer;
- bonding the substrate and the wafer such that the oxide layer and the said top layer are at the bonding interface,
- reducing the wafer for only leaving the top layer bonded to the substrate via the oxide layer: forming thus said structure,
- heat treating this structure for reinforcing the bonding.

Different techniques have been developed nowadays to reduce the wafer, such as Smart Cut™ (whose general description is fully explained in the publication SILICON-ON-INSULATOR TECHNOLOGY: Materials to VLSI, 2nd Edition (Jean-Pierre COLINGE) or BESOI (Bond Etch Silicon On Insulator).

The structure finally obtained comprises the top layer on the oxide layer on the substrate.

The top layer might be made of sapphire, Si <111>, SiC or any other semiconductor material that insures the quality of a growth of a useful layer thereon, e.g. made of a material for high frequency components like GaN.

Additionally, the substrate is chosen for having high heat dissipation properties – i.e. a high thermal conductivity – in order to dissipate the heat produced by the components.

Since the crystal quality of the useful layer during growth on the composite structure is insuring by the top layer, it is not necessary providing the substrate with a high crystal quality. It is for example possible providing a substrate made of a polycrystalline material, like polycrystalline SiC ("polySiC").

These kinds of composite structures are therefore less costly than those of single-crystal SiC while still being a good substrate for the growth of a subsequent useful layer and still having good heat dissipation properties.

But some designed components still require a better heat dissipation.

A purpose of the invention is to increase again such heat dissipation while still fabricating a structure at low cost.

In order to reach this purpose and overcome the drawbacks of the prior art, the invention proposes, according to a first aspect, a method for fabricating a composite structure having high heat dissipation properties, the structure

comprising a support substrate, a top layer and an oxide layer between the support substrate and the top layer, the method comprising the steps of:

a) providing a top layer made of a crystalline material,

b) bonding the top layer with a support substrate made of a polycrystalline material having a heat dissipation properties greater than a bulk single crystal silicon substrate having the same dimensions, such that an oxide layer is formed at the bonding interface, in order to obtain said structure,

characterized in that it further comprises a heat treatment of the structure in an inert or reducing atmosphere at a predetermined temperature and a predetermined duration to increase the heat dissipation properties by dissolving at least a part of the oxide layer.

Other optional characteristics of the said method are:

- step b) comprises forming an oxide layer on the substrate and/or on the top layer, and contacting the top layer with the substrate such that the oxide layer(s) is at the interface;
- step a) comprises providing a donor substrate having said top layer therein, and the method further comprises, between step b) and the heat treatment, a reduction of the thickness of the donor substrate for only keeping the top layer bonded to the support substrate;
- before step a), a step of implanting atomic species in the donor substrate for forming a weakness zone beneath the top layer, and said reduction of the donor substrate comprises supplying energy for detaching the top layer from the donor at the weakness zone;
- the thickness of the support substrate is reduced by application of heat treatment and/or chemical treatment and /or application of mechanicals forces (CMP ..) before bonding;
- the predetermined temperature is between 1100°C and 1300°C, preferably between 1200°C and 1300°C;
- the predetermined duration is about two hours;
- the oxide layer after bonding has a thickness between 10 nm and 1000 nm, and more particularly between 25 nm and 50 nm;

- the top layer after transfer has a thickness between 25 nm and 1000 nm, preferably around 100 nm;
- the substrate is of polycrystalline silicon carbide ;
- the heat treatment is under non oxidant atmosphere for example hydrogen or argon atmosphere.

According to a second aspect, the invention proposes a structure having high heat dissipation properties, consisting of:

- a top layer, made of a crystalline material,
- a support substrate made of a polycrystalline material having a thermal conductivity greater than those of a single crystal silicon substrate having the same dimensions.

Optional characteristics of this structure are as follows:

- the support substrate and the top layer are directly contacted;
- the support substrate is of silicon carbide;
- the top layer is of single crystal silicon <111> or SiC;

According to a third aspect, the invention proposes a use of the said structure as a substrate for the crystal growth of at least one layer made of a material for high-frequency applications.

BRIEF DESCRIPTION OF THE FIGURES

Other characteristics, objects, and advantages of the invention will appear clearer in the description below, which is illustrated by the following figures:

Figure 1 shows a schematic cross-section view of structure according to the prior art.

Figures 2A to 2C show the different steps of a process of manufacturing the structure.

Figure 3 shows steps of a process of manufacturing an example of structure.

DETAILED DESCRIPTION OF THE INVENTION

Referring to figure 1, a structure 50 from which the treatment according to the invention will be processed, is shown.

The structure 50 is a composite structure arranged for being highly heat dissipative, i.e. it is able to dissipate more heat than a bulk single crystal structure having the same dimensions.

This structure 50 comprises a support substrate 20, an oxide layer 30 and a semiconductor top layer 10.

The support substrate 20 stiffens the whole structure 50. To this aim, it has a sufficient thickness, typically of hundreds of micrometers.

The support substrate 20 is made of a material having good heat dissipation properties, i.e. it is able to dissipate more heat than a bulk single crystal substrate having the same dimensions. This material is further made of a low cost material, like a material with low crystalline quality. It can be formed of a polycrystalline SiC, polycrystalline Diamond, or other, or of at least two of these materials stacked one onto the other.

The top layer 10 is of at least one crystalline material.

The top layer 10 may be of SiC, Si<111>, or another crystalline material. An advantage of the Si <111> material is that match with GaN lattice and then could be used for future GaN growth .

The top layer 10 may alternatively be of a combination or a superposition of at least two of these materials and/or a superposition of several sub-layers.

The top layer 10 may be adapted for receiving electronic or optoelectronic components or for being a substrate for the subsequent growth of a useful layer, like a useful layer for high-frequency applications.

According to the invention, the top layer 10 is advantageously thin. Its thickness is advantageously less than about 1000 nm. For example, the top layer 10 may have a thickness between around 25 nm and 1000 nm, preferably around 100nm.

The insulating layer 30 is an oxide layer, buried in the structure 50, located between the support substrate 20 and the top layer 10.

The oxide layer 30 is of an oxide of the crystalline material of the top layer 10 and/or of the top part of the support substrate 20.

For example, if the top layer 10 is of silicon, the oxide layer 30 is of SiO_2.

Its thickness may be between less than 50 nm, and more particularly between around 10 nm and 100 nm.

Referring now to figures 2A-2C, the manufacturing of this structure 50 can be done by a wafer bonding technique.

Especially, referring to figure 2A, the manufacturing can be firstly implemented by providing a wafer 70 with the said top layer 10 therein, the top layer 10 lying at the surface of the wafer 70 defining a front layer on a rear portion 60 of the wafer 70.

A second step consists of bonding the wafer 70 to the support substrate 20 such that the top layer 10 is adjacent to the bonding interface.

Advantageously, the bonding is firstly implemented by well-known bonding techniques (see, for example, "Semiconductor Wafer Bonding Science and Technology" by Q.-Y. Tong and U. Gösele – a Wiley Interscience publication, Johnson Wiley & Sons, Inc – for more details). Thus, for example, molecular bonding of hydrophilic surfaces or surfaces rendered hydrophilic may be done.

Well-known cleaning steps may be implemented just before bonding.

Optionally, a plasma treatment of one and/or the other of the two surfaces to be bonded, followed by conventional annealing or RTA treatment (rapid thermal annealing), is implemented.

Before bonding, the oxide layer 30 was formed on the top layer 10 and/or on the substrate 20, for being buried at the bonding interface after bonding.

The oxide layer 30 may be formed by oxidation of the top layer 10 and / or of the substrate 20.

For example, if the top layer 10 is of Si (111) or SiGe (111), SiO_2 layer 30 may be formed at the surface by deposition or thermal oxidation.

Alternatively, the oxide layer 30 may be formed by deposition of aggregates constituted of the oxide material.

For example, SiO_2 aggregates may be deposited.

Alternatively, both surfaces of the top layer 10 and the substrate 20 may also have oxide layer formed thereon either by deposition or by oxidation.

The parameters of the formation of the oxide are controlled such that the oxide layer 30 has a predetermined thickness for being a thermal barrier between the top layer 10 and the substrate 20.

Referring to figure 2B, the substrate 20 and the wafer 70 are bonded together such that the oxide layer 30 is located at their interface, as previously explained.

Optionally, at least one step of heating is additionally implemented for reinforcing the bonds at the interface.

Referring to figure 2C, the wafer 70 is then reduced such that the whole rear portion 60 is removed. Only the top layer 10 is kept.

Any technique of wafer reduction may be used, such as chemical etching technique, lapping then polishing, Smart Cut® technology which is known per se to the skilled person (see for example « Silicon-On-Insulator Technology : Materials to VLSI, 2nd Edition » from Jean-Pierre Colinge in « Kluwer Academic Publishers », p.50 et 51), taken alone or in combination.

In particular, if using the Smart Cut® technology, the wafer 70 is implanted prior to bonding, with atomic species (such as hydrogen, helium or a combination of the two, and/or other atomic species) at energy and dose selected to form therein a zone of weakness at a depth close to the thickness of the top layer 10. The implantation may be carried out before or after forming the thin oxide layer 30. Finally, once the bonding has been carried out, Smart Cut® technology comprises supplying suitable energy (like thermal and/or mechanical energy) for rupturing the bonds at the zone of weakness, and thus detaching the rear portion 60 from the top layer 10.

An optional step of finishing (by polishing, CMP, cleaning, RTA...) may be implemented after the reduction step, in order to have a smooth and homogeneous top layer 10 but also to cure potential defects due to the implantation step.

Other steps may also be provided, with no limitation according to the invention.

The obtained structure 50 comprises successively the top layer 10, the oxide layer 30 and the support substrate 20.

A heat treatment is then implemented in an inert or reducing atmosphere, like argon or hydrogen atmosphere or a mixture of them.

The heat treatment is processed such that the oxide layer 30 reduces in thickness, by oxygen diffusion through the top layer 10. The temperature and the duration of the heat treatment are then chosen for inciting an amount of oxygen of the oxide layer 30 to diffuse through the top layer 10 rather than in the bulk substrate 20.

Additionally, the thickness of the top layer 10 may also have been chosen, when forming it, for inciting the said diffusion. Indeed, the thinner the top layer 10, the faster the diffusion.

This diffusion may also be accelerated by the fact that the atmosphere is chosen inert, as it can be deduced from the boundary conditions.

In particular, the following reaction occurs at the surface of the semiconductor layer 10 if the inert atmosphere contains argon and the top layer 10 is of silicon:

$$Si + O_i \rightarrow SiO\uparrow$$

For increasing the efficiency of this diffusion, a previous deoxidation of the surface of the semiconductor layer 10 may be done.

But the main parameters affecting the time of diffusion is the anneal temperature and the thickness of the top semiconductor layer 10.

For example, the minimum annealing conditions to dissolve 2 nm of interfacial SiO_2, with 100 nm of top Si <111> layer 10, in a Ar or H_2 atmosphere, are:

- 1 100°C for 2hr, or
- 1 200°C for 10 min, or
- 1 250°C for 4 min.

The temperature and the duration of the heat treatment are then chosen for inciting an amount of oxygen of the oxide layer 30 to diffuse through the top layer 10.

Then, the thickness of the oxide layer 30 decreases by a predetermined value.

Additionally, the thickness of the top layer 10 may also have been chosen, when forming it, for inciting the said diffusion.

Particularly, the thickness of the top layer 10 and the temperature of the heat treatment determine the mean reduction rate of the oxide layer 30. More the thickness less the rate. More the temperature more the rate.

For example, said thickness and temperature may be predetermined such that at least about 0.5 angstroms per minute of oxide layer 30 mean reduction rate is reached. To this purpose, for a temperature of about 1200°C, a thickness of a Si single crystal layer 10 is chosen less than 2500 angstroms.

Only the duration of the heat treatment is then necessary to control for accurately reducing the thickness of the oxide layer 30 by a predetermined value.

Alternatively, the thickness of the top layer 10 has been chosen for reducing the oxide layer 30 by a predetermined value by implementing the heat treatment with a predetermined duration and a predetermined temperature.

The predetermined temperature may be chosen about 1000°C – 1300°C, and especially around 1200°C and/or 1300°C.

The thickness of the top layer 10 may be between around 25 and around 1000 nanometers, the predetermined temperature is about 1200°C and the predetermined duration is between around 5 minutes and 5 hours.

The heat treatment may be processed for removing the whole oxide layer 30 or a part of it.

The final structure 50 after this heat treatment does not comprise some oxide layer 20 any longer or comprises a thinner oxide layer 20 between the top layer 10 and the substrate 20. Due to the low heat dissipation of an oxide material, the heat dissipation of the whole structure 50 is improved after having removed at least a part of the oxide layer 30.

Another advantage of the diffusion of oxygen under hydrogen atmosphere is the diffusion of contaminated particles, like boron atoms, trapped at the bonding interface. Indeed, the heat treatment under hydrogen

atmosphere may lead to the diffusion of boron atomes through the top layer 10 and their evaporation at the surface of the top layer 10.

$$2\,B + 3\,H_2 \rightarrow B_2H_6 \uparrow$$

As the boron decreases the resistivity of the HR Silicon, the final structure 50 may have an interface of better quality, with improved electrical properties.

Furthermore, due to the poor crystalline quality of the polycrystalline material of the support substrate 20 and to its thermal conductivity, the final temperature of the heat treatment can be reached with rapid ramps for temperature increase (or decrease) without leading to slip lines formation with a final temperature that could be up to 1300°C. The manufacturing costs are consequently reduced, thanks to the decrease of the time of manufacturing and to the choice of the bulk substrate, while the heat dissipation properties of the final structure 50 are increased.

Finally, the silicon HR (for "High Resistivity") is not necessary. There could also be applications requiring electrical conductance at the substrates and therefore inducing the use of other materials.

Description of a particular embodiment

Referring to figure 3, a polySiC substrate 20 is bonded to a Si (111) wafer 70.

The oxide layer 30 is formed on the silicon wafer 70 and/or on the polySiC substrate 20. The oxide layer 30 on the wafer 70 is formed thermally or by deposition, while the oxide layer 30 on the polySiC is formed by deposition by PECVD (Plasma-Enhanced Chemical Vapor Deposition) or LPCVD (Low Pressure Chemical Vapor Deposition). The thickness of the global oxide layer, which is here SiO_2, is between around 25 nm and around 50 nm.

The Smart Cut® implantation of the donor substrate 20 prior to the bonding leads to the formation of a weakness zone 15. Then, the transfer of a thin Si (111) layer 10 to the substrate 20 is obtained after application of mechanical forces and/or by heating in order to break the mechanical bonds at the weakness zone 15.

As polySiC may be rough for bonding, the LPCVD oxide 30 is preferably polished to reduce such roughness before being bonded to the Si (111) wafer 70.

The bonding is obtained by molecular bonding and the interface is reinforced by a thermal treatment. This thermal treatment is also used for dissolving the insulating layer 30 by diffusion of oxygen. This thermal treatment is realized at a temperature comprised between 1150°C and 1250°C, more precisely 1200 °C, for around five minutes to five hours (preferably, for 2 hours), under an atmosphere comprising hydrogen or argon, or a mixture of both.

As a result, the oxide layer 30 is entirely dissolved.

Claims

1. Method for fabricating a composite structure having high heat dissipation properties, the structure comprising a support substrate, a top layer and an oxide layer between the support substrate and the top layer, the method comprising the steps of:

a) providing a top layer made of a crystalline material,

b) bonding the top layer with a support substrate made of a polycrystalline material having a heat dissipation properties greater than a bulk single crystal silicon substrate having the same dimensions, such that an oxide layer is formed at the bonding interface, in order to obtain said structure,

characterized in that it further comprises a heat treatment of the structure in an inert or reducing atmosphere at a predetermined temperature and a predetermined duration to increase the heat dissipation properties by dissolving at least a part of the oxide layer.

2. Method for fabricating a composite structure according to the preceding claim, wherein step b) comprises forming an oxide layer on the substrate and/or on the top layer, and contacting the top layer with the substrate such that the oxide layer(s) is at the interface.

3. Method for fabricating a composite structure according to any one of the preceding claims, wherein step a) comprises providing a donor substrate having said top layer therein, wherein the method further comprises, between step b) and the heat treatment, a reduction of the thickness of the donor substrate for only keeping the top layer bonded to the support substrate.

4. Method for fabricating a composite structure according to any one of the preceding claims, wherein before step a), a step of implanting atomic species in the donor substrate for forming a weakness zone beneath the top layer, and wherein said reduction of the donor substrate comprises supplying energy for detaching the top layer from the donor at the weakness zone.

5. Method for fabricating a composite structure according to any one of the preceding claims, wherein the thickness of the support substrate is reduced before bonding.

6. Method for fabricating a composite structure according to any one of the preceding claims, wherein the predetermined temperature is between 1100°C and 1300°C, preferably between 1200°C and 1300°C.

7. Method for fabricating a composite structure according to any one of the preceding claims, wherein the predetermined duration is about two hours.

8. Method for fabricating a composite structure according to any one of the preceding claims, wherein the oxide layer after bonding has a thickness between 10 nm and 1000 nm.

9. Method for fabricating a composite structure according to any one of the preceding claims, wherein the oxide layer after bonding has a thickness between 25 nm and 50 nm.

10. Method for fabricating a composite structure according to any one of the preceding claims, wherein the top layer after transfer has a thickness between 25 nm and 1000 nm, preferably around 100 nm.

11. Method for fabricating a composite structure according to any one of the preceding claims, wherein the substrate is of polycrystalline silicon carbide.

12. Method for fabricating a composite structure according to any one of the preceding claims, wherein the top layer is made of silicon carbide.

13. Method for fabricating a composite structure according to any one of preceding claims, wherein the top layer is made of silicon <111>.

14. Method for fabricating a composite structure according to any one of the preceding claims, wherein the heat treatment is under hydrogen atmosphere.

15. Method for fabricating a composite structure according to any one of the preceding claims, wherein the heat treatment is under argon atmosphere.

16. Structure having high heat dissipation properties, consisting of:

- a top layer, made of a crystalline material,
- a support substrate made of a polycrystalline material having a thermal conductivity greater than those of a single crystal silicon substrate having the same dimensions.

17. Structure according to the preceding claim, characterized in that the support substrate and the top layer are directly contacted.

18. Substrate with a multilayer semiconductor structure according to anyone of the two preceding claims, wherein the support substrate is of silicon carbide.

19. Semiconductor structure according to anyone of the three preceding claims, wherein the top layer is of single crystal silicon <111> or SiC.

20. Use of the structure according to one of the four preceding claims as a substrate for the crystal growth of at least one layer made of a material for high-frequency applications.