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(54) SYNCHRONIZED TIME DELAY CIRCUITS

(71) We, HEWLETT-PACKARD COMPANY, of 1501 Page Mill Road, Palo Alto, California, United States of America, a corporation organized and existing under the laws of the State of California, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to synchronized time delay circuits and more particularly to an improved and simplified version thereof. These types of circuits have been used to provide an output pulse delayed from the time of application of a trigger voltage and in synchronization with a pulse externally supplied, typically at the input. The problems encountered with previous circuits have been susceptibility to reset from the synchronizing pulses, high quiescent power consumption, and high component count.

It is an object of the present invention to provide an improved synchronized time delay circuit.

The present invention provides a synchronized time delay circuit comprising a transistorized Schmitt trigger circuit having an input and an output; means for applying a gradually increasing voltage at the input, and means for applying synchronization pulses at the output so that a unilateral pulse appears at the output when the combined magnitudes of the input voltage and of at least a portion of a synchronization pulse exceed a predetermined threshold voltage level, thereby preventing subsequent synchronization pulses from changing the state of the Schmitt trigger circuit.

Preferably the means for applying a gradually increasing voltage at the input comprises a resistor-capacitor integrating network switchably connected between a source of D.C. potential and a source of reference potential and additionally connected to the input of the Schmitt trigger circuit.

Preferably the Schmitt trigger circuit comprises input and output transistors, the base of the input transistor being the input of the Schmitt trigger circuit, the emitters of

the input and output transistors being commoned and returned through a resistor to a source of reference potential, the collectors of the input and output transistors being returned through separate resistors to a source of operating potential, the collector of the input transistor being connected to the base of the output transistor, and the collector of the output transistor being the output of the Schmitt trigger circuit.

Preferably said means for applying synchronization pulses includes a resistor connected to the collector of the output transistor of the Schmitt trigger circuit for applying synchronization pulses thereto.

This invention provides a circuit for providing a unilateral output voltage step which disconnects the synchronizing trigger to guarantee stability. The invention also provides a circuit having low quiescent power consumption, in contemplation of its possible operation from a battery power supply, and a small number of components.

There now follows a description which is to be read with reference to the accompanying drawings of a circuit according to the invention; it is to be clearly understood that the circuit has been selected for description to illustrate the invention by way of example.

In the drawings:—

Fig. 1 is a schematic diagram of a circuit according to the invention;

Figs. 2 (A)—(C) show typical input, output, and synchronization pulse waveforms as functions of time.

Fig. 1 shows a synchronized time delay circuit utilizing a Schmitt trigger flip flop 8 comprising transistors 10 and 12, the emitters of which are commoned and connected through a resistor 14 to a source of reference potential, such as ground potential, and the collectors of which are returned through resistors 16 and 18 to a source of operating potential at a terminal 20. The resistor 18 is connected to the base of the transistor 12 for the purpose of providing a base current path to maintain the transistor 12 in an "on" state, thereby holding the collector of the transistor 12, and hence the output of the synchronized time delay circuit, near ground potential. A switch 22 is connected

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to the source at the terminal 20 of operating potential and is also serially connected through a resistor 24 to the base of the transistor 10, which base is also connected
 5 through a capacitor 26 to the source of reference potential. Closure of the switch 22 allows the base voltage of the transistor 10 to increase gradually, as shown in Fig. 2(A), toward a predetermined threshold
 10 voltage level, defined by the base-emitter voltage of the transistor 10 and the voltage drop produced by current flowing through the resistor 14. Synchronization pulses 30, such as those shown in Fig. 2(C), are injected through a resistor 28 to the output
 15 of the synchronized time delay circuit at the collector of the transistor 12. When the combined magnitudes of the base voltage of the transistor 10 and of at least a portion
 20 of the negative going transition voltage of a synchronization pulse as determined by the division ratio of the resistors 28 and 14 exceed the threshold voltage, the transistor 10 turns on and the transistor 12 turns off.
 25 At this time the collector of the transistor 12 assumes the operating potential value, thereby forming the output voltage step as shown in Fig. 2(B). Further application of synchronization pulses 30 has a negligible effect
 30 on the voltage at a synchronized delay output 32.

WHAT WE CLAIM IS:—

1. A synchronized time delay circuit
 35 comprising a transistorized Schmitt trigger circuit having an input and an output; means for applying a gradually increasing voltage at the input; and means for applying synchronization pulses at the output so that a
 40 unilateral pulse appears at the output when the combined magnitudes of the input voltage and of at least a portion of a synchronization pulse exceed a predetermined threshold voltage level, thereby preventing
 45 subsequent synchronization pulses from

changing the state of the Schmitt trigger circuit.

2. A synchronized time delay circuit according to claim 1 wherein the means for
 50 applying a gradually increasing voltage at the input comprises a resistor-capacitor integrating network switchably connected between a source of D.C. potential and a source of reference potential and additionally
 55 connected to the input of the Schmitt trigger circuit.

3. A synchronized time delay circuit according to any one of claims 1 and 2 wherein the Schmitt trigger circuit comprises input and output transistors the base
 60 of the input transistor being the input of the Schmitt trigger circuit, the emitters of the input and output transistors being commoned and returned through a resistor to a source of reference potential, the collectors of the
 66 input and output transistors being returned through separate resistors to a source of operating potential, the collector of the input transistor being connected to the base of the output transistor, and the collector of
 70 the output transistor being the output of the Schmitt trigger circuit.

4. A synchronized time delay circuit according to claim 3 wherein said means
 75 for applying synchronization pulses includes a resistor connected to the collector of the output transistor of the Schmitt trigger circuit for applying synchronization pulses thereto.

5. A synchronized time delay circuit
 80 according to claim 1 substantially as hereinbefore described with reference to the accompanying drawings.

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to the source at the terminal 20 of operating potential and is also serially connected through a resistor 24 to the base of the transistor 10, which base is also connected through a capacitor 26 to the source of reference potential. Closure of the switch 22 allows the base voltage of the transistor 10 to increase gradually, as shown in Fig. 2(A), toward a predetermined threshold voltage level, defined by the base-emitter voltage of the transistor 10 and the voltage drop produced by current flowing through the resistor 14. Synchronization pulses 30, such as those shown in Fig. 2(C), are injected through a resistor 28 to the output of the synchronized time delay circuit at the collector of the transistor 12. When the combined magnitudes of the base voltage of the transistor 10 and of at least a portion of the negative going transition voltage of a synchronization pulse as determined by the division ratio of the resistors 28 and 14 exceed the threshold voltage, the transistor 10 turns on and the transistor 12 turns off. At this time the collector of the transistor 12 assumes the operating potential value, thereby forming the output voltage step as shown in Fig. 2(B). Further application of synchronization pulses 30 has a negligible effect on the voltage at a synchronized delay output 32.

WHAT WE CLAIM IS:—

1. A synchronized time delay circuit comprising a transistorized Schmitt trigger circuit having an input and an output; means for applying a gradually increasing voltage at the input; and means for applying synchronization pulses at the output so that a unilateral pulse appears at the output when the combined magnitudes of the input voltage and of at least a portion of a synchronization pulse exceed a predetermined threshold voltage level, thereby preventing subsequent synchronization pulses from

changing the state of the Schmitt trigger circuit.

2. A synchronized time delay circuit according to claim 1 wherein the means for applying a gradually increasing voltage at the input comprises a resistor-capacitor integrating network switchably connected between a source of D.C. potential and a source of reference potential and additionally connected to the input of the Schmitt trigger circuit.

3. A synchronized time delay circuit according to any one of claims 1 and 2 wherein the Schmitt trigger circuit comprises input and output transistors the base of the input transistor being the input of the Schmitt trigger circuit, the emitters of the input and output transistors being commoned and returned through a resistor to a source of reference potential, the collectors of the input and output transistors being returned through separate resistors to a source of operating potential, the collector of the input transistor being connected to the base of the output transistor, and the collector of the output transistor being the output of the Schmitt trigger circuit.

4. A synchronized time delay circuit according to claim 3 wherein said means for applying synchronization pulses includes a resistor connected to the collector of the output transistor of the Schmitt trigger circuit for applying synchronization pulses thereto.

5. A synchronized time delay circuit according to claim 1 substantially as hereinbefore described with reference to the accompanying drawings.

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