

WHAT IS CLAIMED IS:

1. A chip frequency modulation method of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, comprising steps of:

setting a plurality of working frequencies of each of the plurality of cores the operational chip of the computing device and causing each of the plurality of cores in the operational chip to work at a current working frequency to compute one or more Nonces, wherein the current working frequency is one of the plurality of working frequencies;

receiving, from each of the plurality of cores, the one or more Nonces computed at the current working frequency;

for each of the plurality of cores, analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency; and

for at least one of the plurality of cores, modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator .

2. The chip frequency modulation method according to claim 1, wherein the step of setting a plurality of working frequencies of each of the plurality of cores the operational chip of the computing device and causing each of the plurality of cores in the operational chip to work at a current working frequencies further comprises:

setting the plurality of working frequencies for the operational chip through a plurality of phase locked loops, the working frequencies and the phase locked loops being in a one-to-one correspondence relationship;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

modulating the current working frequency up or down through the phase locked loops according to the computing performance indicator .

3. The chip frequency modulation method according to claim 2, wherein the phase locked loops are provided inside or outside the operational chip.

4. The chip frequency modulation method according to claim 1, wherein a frequency difference between the adjacent working frequencies is from 1% to 10%.

5. The chip frequency modulation method according to claim 1, wherein the step of analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency further comprises:

analyzing whether the computing performance indicator reaches a first, second and/or third indicator thresholds within a modulation period, the first indicator threshold being the same as or different from the second indicator threshold;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

if the computing performance indicator reaches the first indicator threshold, modulating the current working frequency up to an upper working frequency of the plurality of working frequencies that is higher than the current working frequency;

if the computing performance indicator does not reach the second indicator threshold, modulating the current working frequency down to a lower working frequency of the plurality of working frequencies that is lower than the current working frequency; and/or

if the computing performance indicator reaches the third indicator threshold, modulating the current working frequency down to the lower working frequency.

6. The chip frequency modulation method according to claim 1, further comprising:

if a portion of the cores worked at one or more optimized working frequencies exceed a first ratio, stopping modulating frequencies of the cores; or

if a portion of the cores worked at the one or more optimized working frequencies is majority, stopping modulating the frequencies of the cores.

7. The chip frequency modulation method according to claim 1, wherein the step of analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency further comprises:

analyzing whether a computing correct ratio of the core reaches a first and/or second correct ratio thresholds within a modulation period, the first correct ratio threshold being the same or different from the second correct ratio threshold;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

if the computing correct ratio reaches the first correct ratio threshold, modulating the current working frequency up to an upper working frequency of the plurality of working frequencies that is higher than the current working frequency; and/or

if the computing correct ratio does not reach the second correct ratio threshold, modulating the current working frequency down to a lower working frequency of the plurality of working frequencies that is lower than the current working frequency.

8. The chip frequency modulation method according to claim 7, wherein the step of analyzing whether a computing correct ratio reaches the first and/or second correct ratio thresholds within a modulation period further comprises:

analyzing whether random numbers submitted by the at least one core are correct within the modulation period;

counting a number of correct random numbers and a number of wrong random numbers of the core within the modulation period;

computing a computing correct ratio of the random numbers within the modulation period according to the number of correct random numbers and the number of wrong random numbers, and judging whether the computing correct ratio of the random numbers reaches the first and/or second correct ratio thresholds;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

if the computing correct ratio of the random numbers reaches the first correct ratio threshold, modulating the current working frequency of the core up to the upper working frequency;

if the computing correct ratio of the random numbers does not reach the second correct ratio threshold, modulating the current working frequency of the core down to the lower working frequency.

9. The chip frequency modulation method according to claim 8, wherein the step of analyzing whether random numbers submitted by the at least one core are correct within the modulation period further comprises:

computing, via the at least one core, a first result from the random numbers through an algorithm when the core submits one random number within the modulation period, the first result including a first feature;

computing, via a verification unit of the operational chip, a second result from the random numbers through the same algorithm, the second result including a second feature;

if the first feature is the same as the second feature, judging, via the verification unit, that the random numbers are the correct random numbers, or when the first feature is not the same as the second feature, judging that the random numbers are the wrong random numbers.

10. The chip frequency modulation method according to claim 7, wherein the step of analyzing whether a computing correct ratio of the core reaches a first or second correct ratio thresholds within a modulation period further comprises:

real-time analyzing whether the computing correct ratio within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a preset real-time modulating instruction;

analyzing whether the computing correct ratio within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a preset

timed modulating instruction within a modulation time period set by the timed modulating instruction; or

analyzing whether the computing correct ratio within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a received immediate modulating instruction;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

if the computing correct ratio within the modulation period reaches the first correct ratio threshold, real-time modulating the current working frequency up to the upper working frequency; if the computing correct ratio within the modulation period does not reach the second correct ratio threshold, real-time modulating the current working frequency down to the lower working frequency;

if the computing correct ratio within the modulation period reaches the first correct ratio threshold in the modulation time period, modulating the current working frequency up to the upper working frequency; if the computing correct ratio within the modulation period does not reach the second correct ratio threshold in the modulation time period, modulating the current working frequency down to the lower working frequency; or

according to the received immediate modulating instruction, if the computing correct ratio within the modulation period reaches the first correct ratio threshold, modulating the current working frequency up to the upper working frequency; if the computing correct ratio within the modulation period does not reach the second correct ratio threshold, modulating the current working frequency down to the lower working frequency; according

to a received stop modulating instruction, stopping modulating the current working frequency .

11. The chip frequency modulation method according to claim 1, wherein the step of analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency further comprises:

presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core;

analyzing whether each computation of the at least one core is correct;

adding a computing correct weight value to a reference node value every time when the at least one core computes correctly at least once, and deducting a computing wrong weight value from the reference node value every time when the at least one core computes wrongly at least once;

judging whether a current reference node value of the at least one core reaches a computing correct threshold or a computing wrong threshold;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

if the current reference node value reaches the computing correct threshold, modulating the current working frequency of the core up to an upper working frequency of the plurality of working frequencies that is higher than the current working frequency; or;

if the current reference node value reaches the computing wrong threshold, modulating the current working frequency of the core down to a lower working frequency of the plurality of working frequencies that is lower than the current working frequency.

12. The chip frequency modulation method according to claim 11, wherein the step of analyzing whether each computation of the at least one core is correct further comprises:

analyzing whether the random numbers submitted every time by the at least one core are correct;

the step of adding one computing correct weight value to the reference node value every time when the at least one core computes correctly at least once, and reducing one computing wrong weight value from the reference node value every time when the core computes wrongly at least once further comprises:

adding one computing correct weight value to the reference node value every time when the core submits at least one correct random number, and reducing one computing wrong weight value from the reference node value every time when the at least one core submits at least one wrong random number.

13. The chip frequency modulation method according to claim 12, wherein the step of analyzing whether the random numbers submitted every time by the at least one core are correct further comprises:

computing, via the at least one core, a first result from the random numbers through a predetermined algorithm after the core submits one random number, the first result including a first feature;

computing, via a verification unit of the operational chip, a second result from the random numbers through the same algorithm, the second result including a second feature;

if the first feature is the same as the second feature, judging, via the verification unit, that the random numbers are the correct random numbers, or the random numbers are the wrong random numbers.

14. The chip frequency modulation method according to claim 11, wherein the method further comprises:

setting and adjusting the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing wrong threshold according to actual requirements, the computing correct weight value being the same as or different from the computing wrong weight value, the computing correct threshold being the same as or different from the computing wrong threshold;

controlling an expected tolerant resident error ratio by controlling a ratio of the computing correct weight value to the computing wrong weight value;

controlling a modulation period by controlling an absolute value of the computing correct weight value and the computing wrong weight value;

controlling the modulation period by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

15. The chip frequency modulation method according to claim 14, wherein a computing formula of the resident error ratio is: the resident error ratio = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

16. The chip frequency modulation method according to claim 11, wherein the step of judging whether a current reference node value of the at least one core reaches a computing correct threshold or a computing wrong threshold further comprises:

real-time judging whether the current reference node value of the at least one core reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction;

judging whether the current reference node value of the at least one core reaches the computing correct threshold or the computing wrong threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

analyzing whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction;

the step of modulating the current working frequency up or down according to the computing performance indicator further comprises:

if the current reference node value of the at least one core reaches the computing correct threshold, real-time modulating the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold, real-time modulating the current working frequency down to the lower working frequency;

if the current reference node value reaches the computing correct threshold in the modulation time period, modulating the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold in the modulation time period, modulating the current working frequency down to the lower working frequency; or

according to the received immediate modulating instruction, if the current reference node value reaches the computing correct threshold, modulating the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold, modulating the current working frequency down to the lower working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency .

17. The chip frequency modulation method according to claim 1, after the step of modulating the current working frequency up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator , further comprising:

counting current distribution state after frequency modulation at the working frequencies;

modulating a frequency in the working frequency according to the current distribution state and a frequency modulation mechanism of the cores, the frequency modulation mechanism being a correspondence relationship between the distribution state and the frequency modulation of the cores.

18. The chip frequency modulation method according to claim 17, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

the step of modulating a frequency in the working frequency according to the current distribution state and a frequency modulation mechanism of the cores further comprises:

if the cores exceeding a second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

if the cores exceeding a third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

19. The chip frequency modulation method according to claim 18, wherein the step of if the cores exceeding the second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency further comprises:

if the cores exceeding the second ratio are worked at the maximum working frequency, modifying the one working frequency to the one optimized high-frequency working frequency; and/or

the step of if the cores exceeding the third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency further comprises:

if the cores exceeding the third ratio are worked at the minimum working frequency, modifying the one working frequency to the one optimized low-frequency working frequency.

20. The chip frequency modulation method according to claim 17, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

the step of modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism further comprises:

if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

21. The chip frequency modulation method according to claim 20, wherein the step of if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency further comprises:

if the number of cores worked at the maximum working frequency is maximum, modifying the one working frequency to the one optimized high-frequency working frequency; and/or

the step of if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency further comprises:

if the number of cores worked at the minimum working frequency is maximum, modifying the one working frequency to the one optimized low-frequency working frequency.

22. The chip frequency modulation method according to claim 17, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency;

the step of modulating a frequency in the working frequency according to the current distribution state and a frequency modulation mechanism further comprises:

if the cores exceeding the fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or

if the number of cores worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency.

23. A chip frequency modulation apparatus of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, comprising:

a frequency setting module for setting a plurality of working frequencies of each of the plurality of cores of the operational chip of the computing device and causing each of the plurality of cores in the operational chip to work a current working frequency to compute one or more Nonces, wherein the current working frequency is one of the plurality of working frequencies;

receiving, from each of the plurality of cores, the one or more Nonces computed at the current working frequency;

a computational performance analysis module for each of the plurality of cores, analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency; and

a frequency modulation module for at least one of the plurality of cores, modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator .

24. The chip frequency modulation apparatus according to claim 23, wherein the frequency setting module sets the plurality of working frequencies for the operational chip through a plurality of phase locked loops, the working frequencies and the phase locked loops being in a one-to-one correspondence relationship;

the frequency modulation module modulates the current working frequency up or down through the phase locked loops according to the computing performance indicator .

25. The chip frequency modulation apparatus according to claim 24, wherein the phase locked loops are provided inside or outside the operational chip.

26. The chip frequency modulation apparatus according to claim 23, wherein a frequency difference between the adjacent working frequencies is from 1% to 10%.

27. The chip frequency modulation apparatus according to claim 23, wherein the computational performance analysis module analyzes whether the computing performance

indicator reaches a first, second and/or third indicator thresholds within a modulation period, the first indicator threshold being the same as or different from the second indicator threshold;

if the computing performance indicator reaches the first indicator threshold, the frequency modulation module modulates the current working frequency up to an upper working frequency;

if the computing performance indicator does not reach the second indicator threshold, the frequency modulation module modulates the current working frequency down to the lower working frequency; and/or

if the computing performance indicator reaches the third indicator threshold, the frequency modulation module modulates the current working frequency of the at least one core down to the lower working frequency.

28. The chip frequency modulation apparatus according to claim 23, wherein the frequency modulation module further comprises:

a frequency modulation sub-module for modulating the current working frequency up or down according to the computing performance indicator ;

a stop frequency modulation sub-module for when a portion of if the cores worked at the predetermined one or more optimized working frequency exceed a first ratio, stopping modulating the frequencies of the cores; or if when a portion of the number of cores worked at the at least one optimized working frequencies is majority, stopping modulating the frequencies of the cores.

29. The chip frequency modulation apparatus according to claim 23, wherein the computational performance analysis module analyzes whether a computing correct ratio

reaches a first and/or second correct ratio thresholds within a modulation period, the first correct ratio threshold being the same or different from the second correct ratio threshold;

the frequency modulation module, if the computing correct ratio reaches the first correct ratio threshold, modulates the current working frequency up to an upper working frequency of the plurality of working frequencies that is higher than the current working frequency;

and/or if the computing correct ratio of the at least one core does not reach the second correct ratio threshold, modulates the current working frequency down to the lower working frequency of the plurality of working frequencies that is higher than the current working frequency.

30. The chip frequency modulation apparatus according to claim 29, wherein the computational performance analysis module further comprises:

a first analysis sub-module for analyzing whether random numbers submitted by the at least one core are correct within the modulation period;

a counting sub-module for counting a number of correct random numbers and a number of wrong random numbers of the core within the modulation period; and

a first judgment module for computing a computing correct ratio of the random numbers within the modulation period according to the number of correct random numbers and the number of wrong random numbers, and judging whether the computing correct ratio of the random numbers reaches the first and/or second correct ratio thresholds;

the frequency modulation module for if the computing correct ratio of the random numbers reaches the first correct ratio threshold, modulating the current working frequency of the core up to the upper working frequency; and/or if the computing correct ratio of the

random numbers does not reach the second correct ratio threshold, modulating the current working frequency of the at least one core down to the lower working frequency.

31. The chip frequency modulation apparatus according to claim 30, wherein the first analysis sub-module further comprises:

a first computing unit for computing a first result from the random numbers through an algorithm when the core submits one random number within the modulation period, the first result including a first feature, the first computing unit provided in the core; and

a first verification unit for computing a second result from the random numbers through the algorithm, the second result including a second feature, if the first feature is the same as the second feature, judging that the random number is the correct random number, or when the first feature is not the same as the second feature. judging that the random number is the wrong random number, the first verification unit provided in the operational chip.

32. The chip frequency modulation apparatus according to claim 29, wherein the computational performance analysis module analyzes whether the computing correct ratio within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a modulating instruction;

the computational performance analysis module analyzes whether the computing correct ratio within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a timed modulating instruction within a modulation time period set by the timed modulating instruction; or

the computational performance analysis module analyzes whether the computing correct ratio within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a received immediate modulating instruction;

the frequency modulation module, if the computing correct ratio within the modulation period reaches the first correct ratio threshold, real-time modulates the current working frequency up to the upper working frequency; if the computing correct ratio within the modulation period does not reach the second correct ratio threshold, modulates the current working frequency down to the lower working frequency;

the frequency modulation module, if the computing correct ratio within the modulation period reaches the first correct ratio threshold in the modulation time period, modulates the current working frequency up to the upper working frequency; if the computing correct ratio within the modulation period does not reach the second correct ratio threshold in the modulation time period, modulates the current working frequency down to the lower working frequency; or

the frequency modulation module, according to the received immediate modulating instruction, if the computing correct ratio within the modulation period reaches the first correct ratio threshold, modulates the current working frequency up to the upper working frequency; if the computing correct ratio within the modulation period does not reach the second correct ratio threshold, modulates the current working frequency down to the lower working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency .

33. The chip frequency modulation apparatus according to claim 23, wherein the computational performance analysis module further comprises:

a setting sub-module for presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core;

a second analysis sub-module for analyzing whether each computation of the at least one core is correct;

a counting sub-module for adding a computing correct weight value to a reference node value every time when the at least one core computes correctly at least once, and deducting computing wrong weight value from the reference node value every time when the at least one core computes wrongly at least once; and

a second judgment sub-module for judging whether the current reference node value of at least one the core reaches the computing correct threshold or a computing wrong threshold;

the frequency modulation module for if the current reference node value reaches the computing correct threshold, modulating the current working frequency of the core up to the upper working frequency of the plurality of working frequencies that is higher than the current working frequency; and if the current reference node value reaches the computing wrong threshold, modulating the current working frequency of the core down to the lower working frequency of the plurality of working frequencies that is lower than the current working frequency.

34. The chip frequency modulation apparatus according to claim 33, wherein the second analysis sub-module analyzes whether the random numbers submitted every time by the core are correct;

the counting sub-module adds one computing correct weight value to the reference node value every time when the core submits at least one correct random number, and

reduces one computing wrong weight value from the reference node value every time when the core submits at least one wrong random number.

35. The chip frequency modulation apparatus according to claim 34, wherein the second analysis sub-module further comprises:

a second computing unit for computing, via the core, a first result from the random number through a predetermined algorithm after the core submits one random number, the first result including a first feature; and

a second verification unit for computing a second result from the random number through the same algorithm, the second result including a second feature; if the first feature is the same as the second feature, judging that the random number is the correct random number, or the random number is the wrong random number.

36. The chip frequency modulation apparatus according to claim 23, wherein the setting sub-module sets and adjusts the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing wrong threshold according to actual requirements, the computing correct weight value being the same as or different from the computing wrong weight value, the computing correct threshold being the same as or different from the computing wrong threshold;

the setting sub-module controls an expected tolerant resident error ratio by controlling a ratio of the computing correct weight value to the computing wrong weight value;

the setting sub-module controls a modulation period by controlling an absolute value of the computing correct weight value and the computing wrong weight value;

the setting sub-module controls the modulation period by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

37. The chip frequency modulation apparatus according to claim 36, wherein a computing formula of the resident error ratio is: the resident error ratio = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

38 The chip frequency modulation apparatus according to claim 33, wherein the computational performance analysis module real-time judges whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction;

the computational performance analysis module judges whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

the computational performance analysis module analyzes whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction;

the frequency modulation module, if the current reference node value reaches the computing correct threshold, real-time modulates the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold, real-time modulates the current working frequency down to the lower working frequency;

the frequency modulation module, if the current reference node value reaches the computing correct threshold in the modulation time period, modulates the current working frequency up to the upper working frequency; if the current reference node value reaches

the computing wrong threshold in the modulation time period, modulates the current working frequency down to the lower working frequency; or

the frequency modulation module, according to the received immediate modulating instruction, if the current reference node value reaches the computing correct threshold, modulates the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold, modulates the current working frequency of the at least one core down to the lower working frequency; according to a received stop modulating instruction, stops modulating the current working frequency of the core.

39. The chip frequency modulation apparatus according to claim 23, further comprising:

a frequency counting module for counting current distribution state of the cores after frequency modulation at the working frequencies;

a frequency modulation module for modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism of the cores, the frequency modulation mechanism being a correspondence relationship between the distribution state and the frequency modulation of the cores.

40. The chip frequency modulation apparatus according to claim 39, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

the frequency modulation module further comprises:

a first frequency modulation sub-module for if the cores exceeding a second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

a second frequency modulation sub-module for if the cores exceeding a third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

41. The chip frequency modulation apparatus according to claim 40, wherein if the cores exceeding the second ratio are worked at the maximum working frequency, the first frequency modulation sub-module modifies the one working frequency to the one optimized high-frequency working frequency; and/or

if the cores exceeding the third ratio are worked at the minimum working frequency, the second frequency modulation sub-module modifies the one working frequency to the one optimized low-frequency working frequency.

42. The chip frequency modulation apparatus according to claim 39, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the

minimum frequency in the low-frequency working frequency is a minimum working frequency;

the frequency modulation module further comprises:

a third frequency modulation sub-module for if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

a fourth frequency modulation sub-module for if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

43. The chip frequency modulation apparatus according to claim 42, wherein if the number of cores worked at the maximum working frequency is maximum, the third frequency modulation sub-module modifies the one working frequency to the one optimized high-frequency working frequency; and/or

if the number of cores worked at the minimum working frequency is maximum, the fourth frequency modulation sub-module modifies the one working frequency to the one optimized low-frequency working frequency.

44. The chip frequency modulation apparatus according to claim 39, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency;

the frequency modulation module further comprises:

a first stop modulation module for if the cores exceeding a fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or

a second stop modulation module for if the number of cores worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency.

45. The chip frequency modulation apparatus according to claim 23, wherein the chip frequency modulation apparatus is provided inside or outside the operational chip.

46. A hash board comprising the chip frequency modulation apparatus according to any one of claims 23 to 45.

47. A computing device comprising the chip frequency modulation apparatus according to any one of claims 23 to 45.

48. A computer program storage medium for storing a computer program, wherein when executed by a processor, the program implements a chip frequency modulation method of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, wherein the method comprises:

setting a plurality of working frequencies of each of the plurality of cores of the operational chip of the computing device and causing each of the plurality of cores in the

operational chip to work at a current working frequency to compute one or more Nonces, wherein the current working frequency is one of the plurality of working frequencies;

receiving, from each of the plurality of cores, the one or more Nonces computed at the current working frequency;

for each of the plurality of cores, analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency; and

for at least one of the plurality of cores, modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator .