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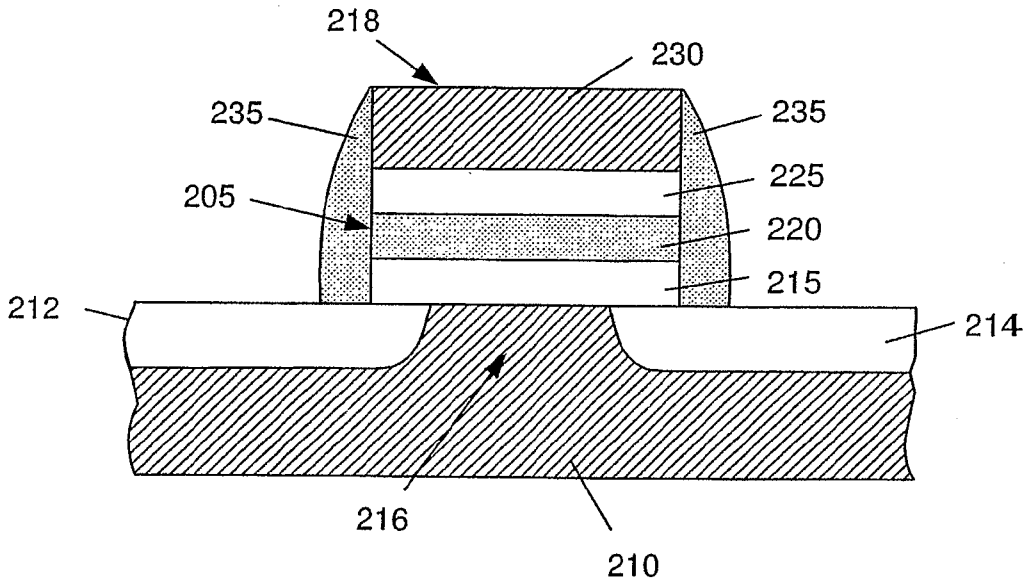
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[Continued on next page]

(54) Title: MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME



(57) Abstract: According to one embodiment, a memory cell structure comprises a semiconductor substrate (210), a first silicon oxide layer (215) situated over the semiconductor substrate, a charge storing layer (220) situated over the first silicon oxide layer, a second silicon oxide layer (225) situated over the charge storing layer, and a gate layer (230) situated over the second silicon oxide layer. In the exemplary embodiment, the charge storing layer (220) comprises silicon nitride having reduced hydrogen content, e.g., in the range of about 0 to 0.5 atomic percent. As a result, the reduced hydrogen content reduces the charge loss in the charge storing layer (220). The reduced charge loss in the charge storing layer (220) has the benefit of reducing threshold voltage shifts, prograirnming data loss, and programming capability loss in the memory device, thereby improving memory device performance.

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