



(51) International Patent Classification:

H01L 21/8238 (2006.01) *H01L 21/768* (2006.01)
H01L 21/311 (2006.01) *H01L 29/49* (2006.01)
H01L 21/02 (2006.01) *H01L 29/66* (2006.01)

(21) International Application Number:

PCT/US2024/020992

(22) International Filing Date:

21 March 2024 (21.03.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

63/454,495 24 March 2023 (24.03.2023) US
18/606,739 15 March 2024 (15.03.2024) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(72) Inventors: **JIANG, Hao**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **KIM, Jong Mun**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **QIAN, Jonathan**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **REN, He**; 3050 Bowers Avenue, Santa Clara, California 95054 (US). **NAIK, Mehul**; 3050 Bowers Avenue, Santa Clara, California 95054 (US).

(74) Agent: **KIMES, Benjamin A.** et al.; Lowenstein Sandler LLP, One Lowenstein Drive, Roseland, New Jersey 07068 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: FABRICATION OF HIGH ASPECT RATIO ELECTRONIC DEVICES WITH MINIMAL SIDEWALL SPACER LOSS

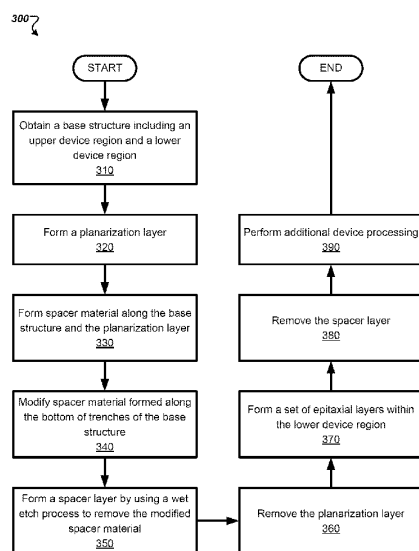


FIG. 3

(57) Abstract: A method includes forming a planarization layer to a position below an upper transistor device region of a base structure of an electronic device and above a lower transistor device region of the base structure. The base structure includes a plurality of features. The method further includes forming spacer material along the base structure and the planarization layer, modifying the spacer material formed along bottom trenches of the base structure to obtain modified spacer material, and forming a spacer layer by using a wet etch process to remove the modified spacer material. Modifying the spacer material formed along the bottom trenches of the base structure to obtain the modified spacer material includes performing a dry etch process targeting the spacer material formed along the bottom trenches of the base structure.

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*